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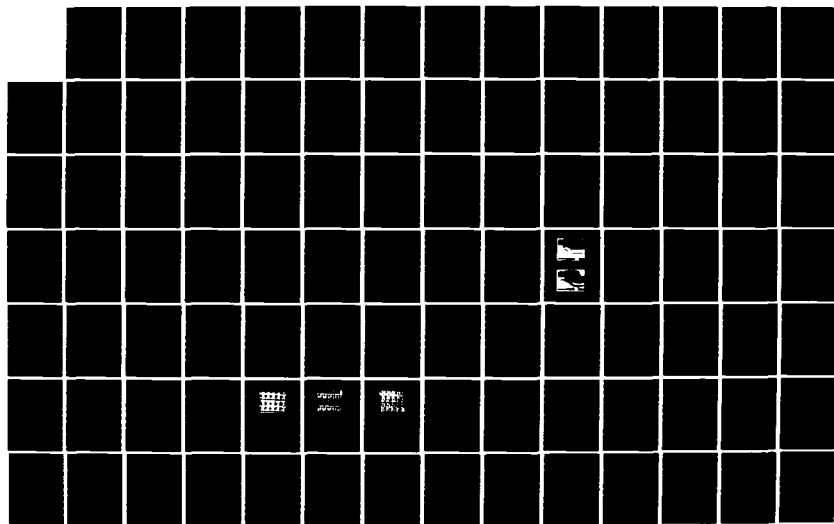
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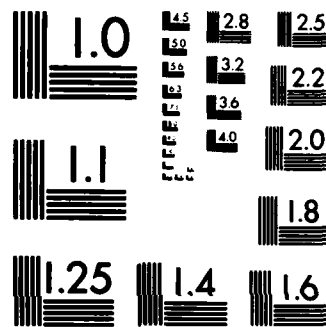
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# STANFORD ELECTRONICS LABORATORIES

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## ANNUAL PROGRESS REPORT NO. 2

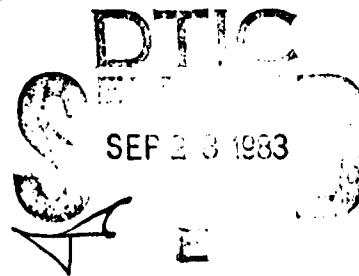
1 April 1982 through 31 March 1983

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# **JSEP Annual Report**

# 1. Very Large Scale Integration

## 1.1 PROPERTIES OF MATERIALS: APPLICATION OF CHANNELING RADIATION TO A STUDY OF THE PROPERTIES OF MATERIALS

*Principal Investigator: R. H. Pantell*

### 1.1.1 Scientific Objectives

The characteristics of the radiation from channeled electrons and positrons are used to investigate the properties of crystals in which the channeling occurs. This provides a new tool for studying defects, measuring thermal vibrational radii, and determining crystalline potential functions. Data are obtained using the 100 MeV electron-positron linear accelerator at the Lawrence Livermore National Laboratory.

### 1.1.2 Progress

During the past year we

- performed measurements of channeling radiation from 54 MeV and 16.9 MeV electrons in LiF;
- investigated the channeling radiation from diamond crystals with and without nitrogen platelet defects;
- compared the channeling radiation in diamond structure crystals, i.e., diamond, silicon and germanium; and
- looked for the effect of gold doping in silicon.

#### 1.1.2.1 Planar and Axial Channeling Radiation from Relativistic Electrons in LiF.

We have measured channeling radiation from the compound binary crystal LiF. This material was chosen because of its low average atomic number (Li,  $Z = 3$  and F,  $Z = 9$ ) and high Debye temperature ( $\approx 730^\circ\text{K}$ ). These properties mean that the scattering of channeled electrons by thermal vibrations of the crystal atoms is relatively small. Other factors in the choice were the availability of high quality samples and the ease of preparation. LiF crystals have the rock salt structure, and for such crystals the planes whose Miller indices are all odd are segregated. That is, there are planes consisting entirely of Li atoms alternating with planes of F atoms. Planes with even indices are mixed, and to first order will appear to a channeled electron to be simple planes of atomic number  $Z = 6$ , the average between Li and F. For axial channeling, the  $\langle 100 \rangle$  and  $\langle 111 \rangle$  axes contain alternate Li and F atoms in a row, whereas the  $\langle 110 \rangle$  axis contains separate rows of Li and F.

Figure 1-1 shows the potential functions and energy eigenvalues (in the laboratory frame) for 16.9 MeV electrons ( $\gamma = 34$ ) axial-channeled by three different axes in LiF. At this energy there are 12 bound states for the  $\langle 100 \rangle$  axis and 8 for the  $\langle 111 \rangle$  axis. For the  $\langle 110 \rangle$  axis there are 21 states for the F strings and 17 for the Li strings. These numbers all are fairly large, so that an absence of distinct lines is expected. The Fourier coefficients of the potentials were obtained from the values of electron-scattering factors for isolated neutral atoms given in [6]. Thermal vibrations were taken into account by the Debye-Waller factor, using a two-dimensional mean-square vibrational amplitude of  $0.141 \text{ \AA}^2$  for both Li and F atoms. The measured axial spectra for 16.9 MeV electrons channeled along the three major axes (with random spectra subtracted), together with the calculated line energies and strengths, are shown in Figure 1-2. It can be seen from this figure that the calculated line energies and strengths correspond remarkably well to the measured spectra. The calculated results for the  $\langle 111 \rangle$  axis in particular (Figure 1-2b), perhaps because this is the simplest case, are seen to be in detailed agreement with the data, with respect to both strength and structure. For this case we can identify the transitions with the spectral lines: the  $2p \rightarrow 1s$  transition gives the highest photon energy (at 33.7 keV); the  $3p \rightarrow 2s$  and  $3s \rightarrow 2p$  transitions produce the spectral peak at 25.3 keV; and the  $3d \rightarrow 2p$  transition gives the lowest photon energy at 20.4 keV. In Figure 1-1, the calculated axial potentials and energy levels for 16.9-MeV electrons in LiF:

- a.) for the  $\langle 100 \rangle$  axis, plotted along the (001) direction;
- b.) for the  $\langle 111 \rangle$  axis, plotted along the (112) direction;
- c.) for the  $\langle 110 \rangle$  axis. In part (c), the interstring position is measured from a point midway between the fluorine string (left) and the lithium string (right), located at  $\sim +0.7 \text{ \AA}$ , respectively. For all three cases, we can identify the lowest, isolated level with the 1s level; the next higher-lying doublet with the 2p and 2s levels (in that order); and the next higher-lying triplet with the 3d, 3s, and 3p levels.

In Figure 1-2, the measured photon spectra (with random spectra subtracted for the 16.9-MeV electrons channeled in LiF) are plotted:

- a) along the  $\langle 100 \rangle$  axis,
- b) along the  $\langle 111 \rangle$  axis
- c) along the  $\langle 110 \rangle$  axis.

The positions of the vertical lines in the Doppler-shifted transition energies between eigenstates of Figure 1-1; their heights indicate the relative intensities of these transitions, assuming equal initial level populations.

In Table 1-1 the measured 54 MeV electron planar channeling radiation peak energies in LiF are

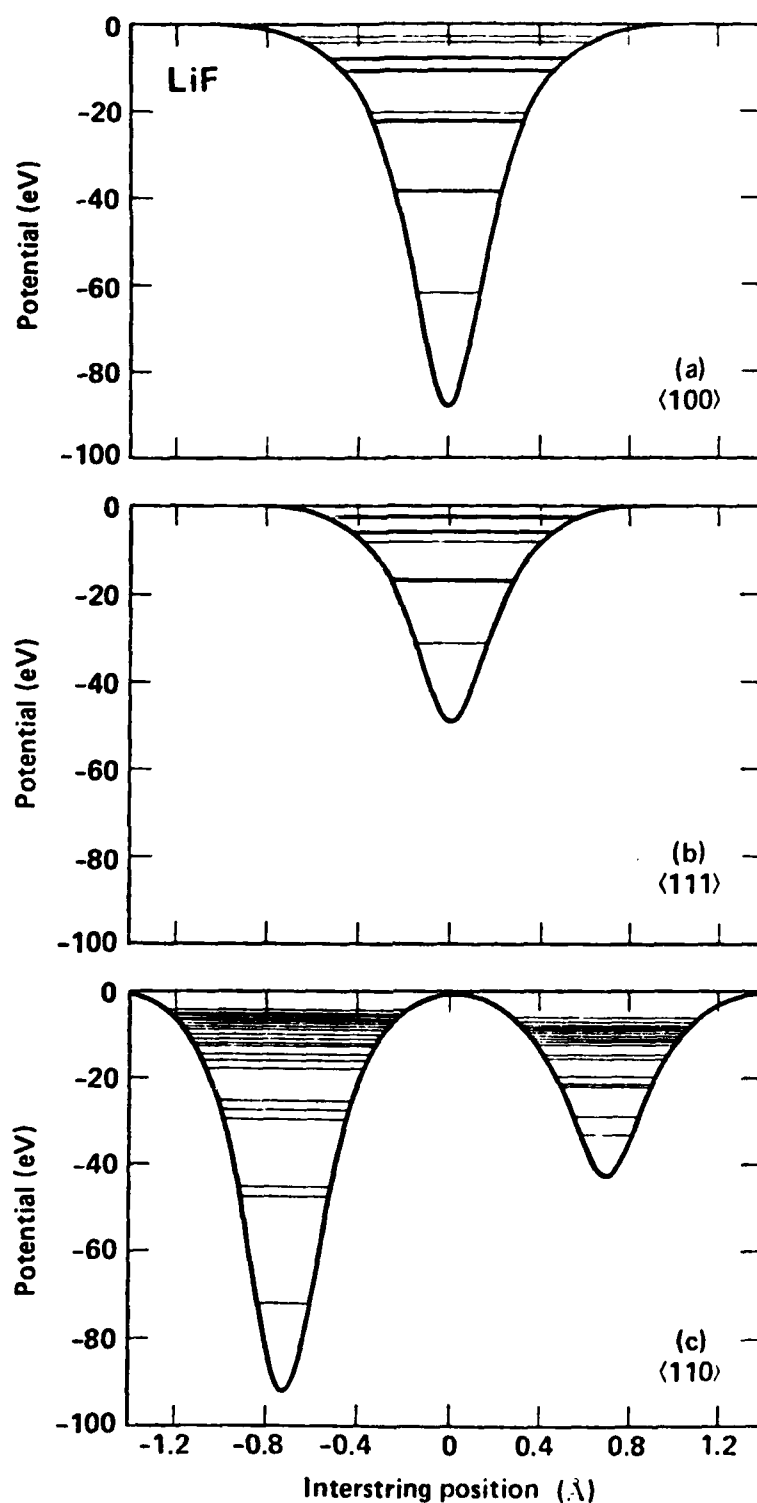


Figure 1-1: Calculated Axial Potentials and Energy Levels for 16.9-MeV Electrons in LiF

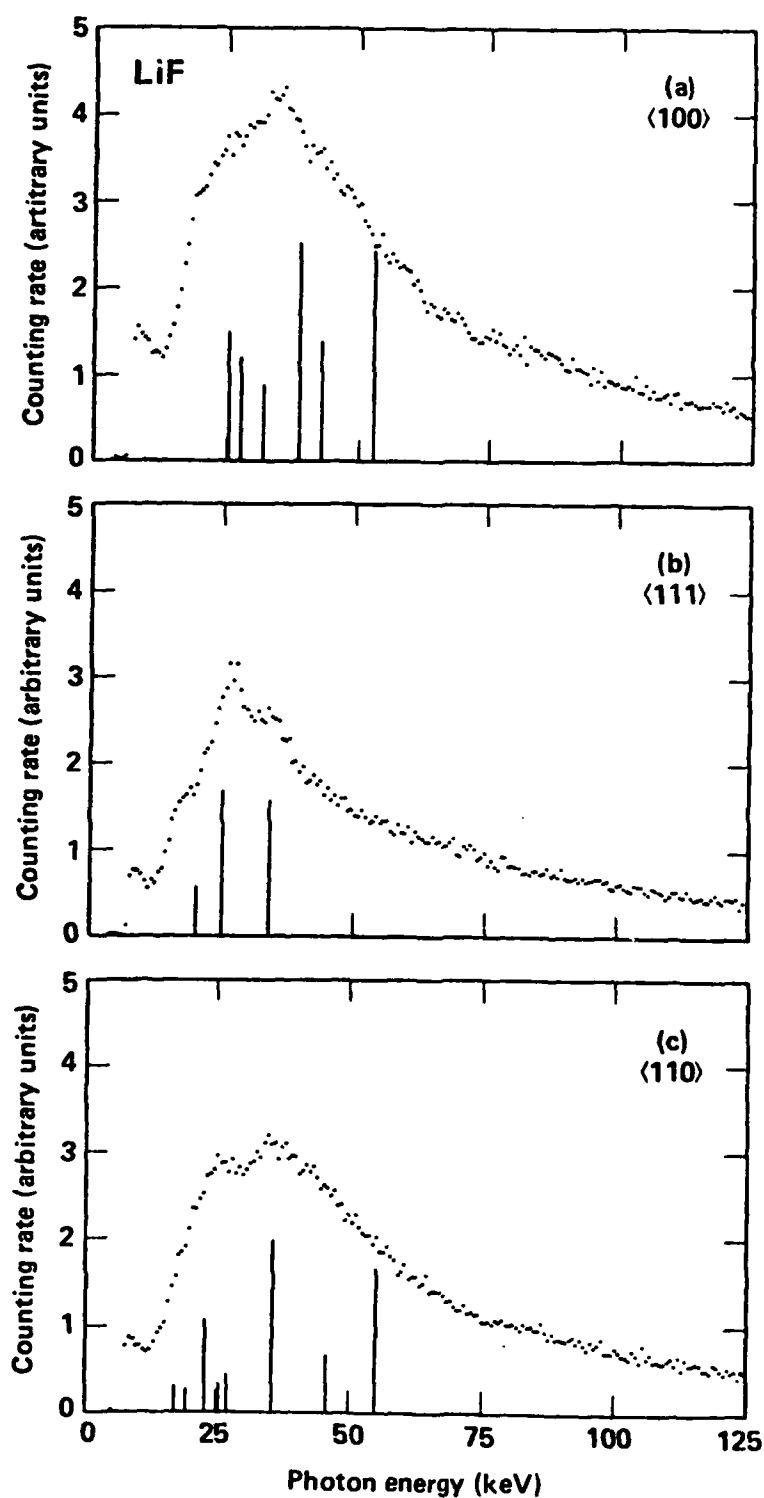


Figure 1-2: Measured photon spectra (with random spectra subtracted for the 16.9-MeV electrons channeled in LiF)

compared with two sets of calculated value: one is calculated with the thermal vibrational radii adjusted to give the best fit to the data, and the other is calculated from tabulated values. The results indicated in Table 1-1 suggest that channeling radiation can be used as a means for determining vibrational radii.

**Table 1-1: Comparison of Calculated and Measured Spectral Line Energies for Electrons Channeled Along Planes in LiF**

Plane	Transition	Measured $\pm 1$	Peak Energy Calculated (a)	Calculated (b)
(100)	1 $\rightarrow$ 0	124.5	124.7	128.9
	2 $\rightarrow$ 1	97.4	97.4	101.5
	3 $\rightarrow$ 2	75.3	75.8	78.4
	4 $\rightarrow$ 3	57.8	59.1	59.7
	5 $\rightarrow$ 4	42.7	45.2	44.4
(110)	1 $\rightarrow$ 0	101.5	101.6	105.1
	2 $\rightarrow$ 1	75.5	75.3	78.2
	3 $\rightarrow$ 2	53.2	53.0	54.3
(111)	1 $\rightarrow$ 0	112.6	112.3	117.1
	2 $\rightarrow$ 1	84.1	84.8	86.4

(a) adjusting thermal vibration radii to give best fit to the data

(b) using tabulated thermal vibrational radii

#### 1.1.2.2 Comparison of Channeling Radiation in Diamonds With and Without Platelet Defects

A possible application for channeling radiation is to study defects and impurities in crystals, and we report [5] the first observations of differences in channeling radiation from planar-channeled positrons and electrons in Type Ia and Type IIa diamonds. Natural diamonds may be classified into four categories: Types Ia, Ib, IIa, and IIb, according to their differences in optical absorption, electron spin resonance spectroscopy, and electrical characteristics [1]. The rarer Type II diamonds exhibit the carbon spectrum consisting of an absorption band between 3 and 6  $\mu\text{m}$ , and an absorption edge in the ultraviolet at 2250 angstrom. Type I diamonds, in addition to the carbon spectrum, have

ultraviolet absorption at 3065 angstrom, and show IR absorption spectrum from  $7.5\text{ }\mu\text{m}$  to  $10\text{ }\mu\text{m}$  due to nitrogen impurities. Some Type II diamonds are found to be p-type semiconductors due to the presence of 0.1 ppm boron and these are classified as Type IIb. Diamonds without the boron impurities are categorized as Type IIa. Type Ib diamonds contain nitrogen in single, substitutional form which can be detected by EST measurements, and Type Ia have their nitrogen in the form of aggregates. These aggregates are responsible for the absorption peaks at  $7.8\text{ }\mu\text{m}$ . Some Type Ia diamonds have an absorption peak of  $7.3\text{ }\mu\text{m}$ , which is related to the presence of platelets precipitated on (100) planes.

In this experiment we used Type Ia and Type IIa diamond crystals, the Type Ia diamond containing nitrogen platelets. These platelets are two layers of nitrogen atoms between (100) planes displacing the lattice on either side, as shown in Figure 1-3 [3]. Along the (100) and (111) planes the platelet appears as a stacking fault, as illustrated in Figures 1-4 and 1-5. In Figure 1-3, the double layer of nitrogen atoms precipitated on the (100) planes constitute a possible scattering center for charged particles channeled along the (100) direction and distort the (100) planes of carbon atoms on both sides of the platelet. The lattice constant  $a = 3.567\text{ angstrom}$ .

In Figure 1-5, the trajectories in the upper part of the figure represent the channeling of positrons, while the trajectories in the lower part of the figure represent the channeling of electrons. Type-IIa diamonds are represented schematically in the left-hand side of the figure. Type-Ia diamonds are represented schematically in the right-hand side of the figure.

A TEM photograph of the Type Ia crystal showed that the platelet diameter varied from 40 to over 200 angstrom, with an average separation of  $\simeq 500\text{ angstrom}$ . From the measured value for the infrared absorption [2], the distance between platelet encounters for a planar-channeled electron or positron is  $\simeq 4500\text{ angstrom}$ .

Channeling radiation experiments were done with 54 MeV electron and positron beams, and Tables 1-2 and 1-3 summarize the results for positron and electron planar channeling, respectively. Type IIa diamond is without the platelets and Type Ia is with the platelets. For positrons in the three major planes the photon energy is constant for both types of diamonds, but there are significant differences in intensity and linewidth.

For positrons in (100) planes, the emission peak near 67 keV almost disappears when platelets are present. This is reasonable, since the platelets distort the existing planes and introduce additional planes which interfere with the channeling.



## Type Ia Platelet

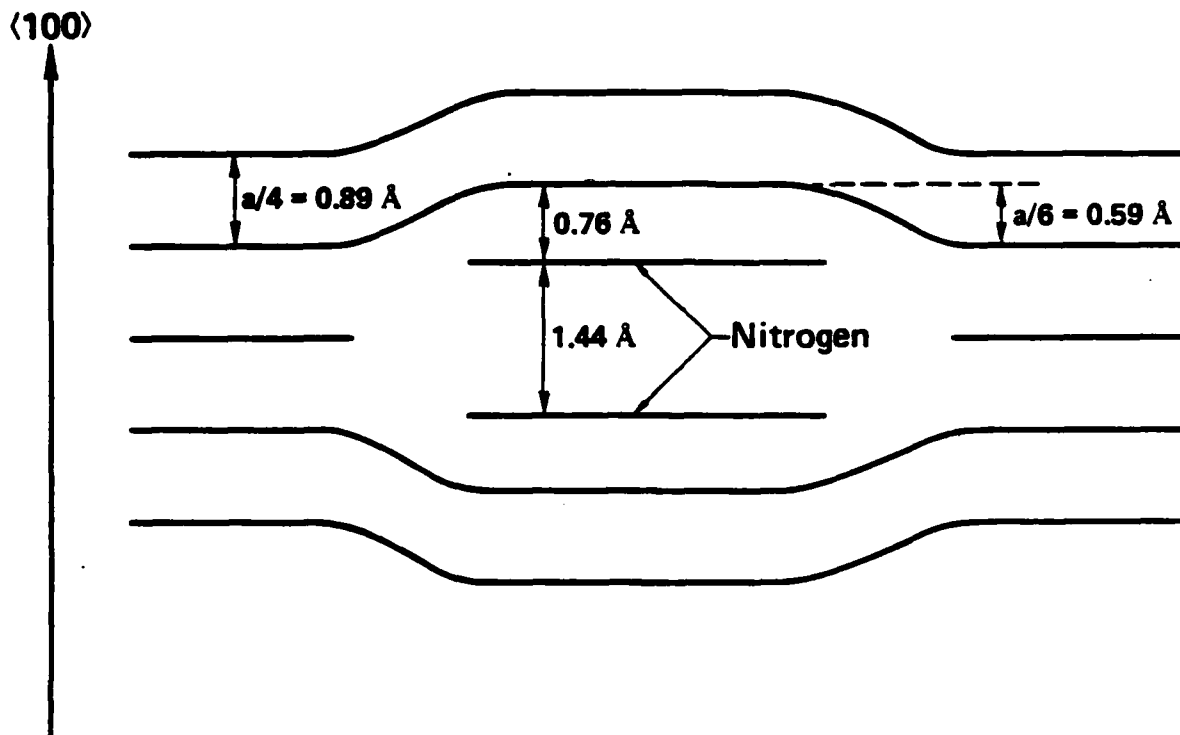


Figure 1-3: Schematic representation of a platelet in a Type-Ia diamond crystal, according to the model [3]

For the (110) and (111) planes, the stacking fault effect is less inhibiting to positron channeling. (Refer to Figures 1-4 and 1-5.) Indeed, for the (111) planes there is only a 42% reduction in the intensity of channeling radiation. In addition, for (111) planes there is also about 40% reduction in linewidth, a result that is contrary to what one would expect from the introduction of a defect. The most likely explanation, which requires further study, is that the stacking fault is preferentially removing population from eigenstates that contribute the most towards line broadening.

For electron channeling radiation, there is no noticeable difference between Type Ia and Type IIa diamonds for (111) planes. For (110) planes almost all the electrons in Type Ia diamond are dechanneled and produce little channeling radiation. Along the (100) planes, the intensities of  $1 \rightarrow 0$  and  $2 \rightarrow 1$  transitions of Type Ia are reduced to about 40% of the Type IIa level, and for both transitions there is a significant increase in linewidth due to the reduced scattering length. A surprising result is the 9 keV reduction in photon energy along (100) planes for the  $1 \rightarrow 0$  transition caused by the introduction of platelets. There is no satisfactory explanation for this observation. We repeated this experiment recently approximately one year after the original observation, and reproduced the results.

(110)

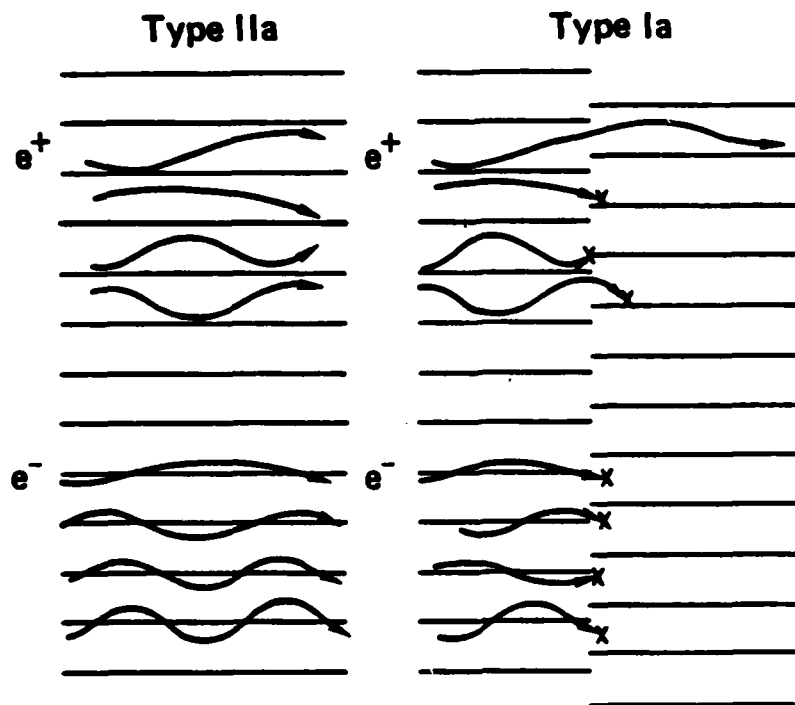


Figure 1-4: Semiclassical interpretation of the channeling of positrons and electrons along the (110) planar direction in Type-IIa and Type-Ia diamonds

#### 1.1.2.3 Channeling Radiation in Si and Gold Doped Si

We measured and compared channeling radiation from 54 MeV electrons and positrons in pure Si and gold doped ( $10^{16} - 10^{17}/\text{cm}^3$ ) Si. The Si crystal was  $19 \mu\text{m}$  thick and gold doped Si was  $40 \mu\text{m}$  thick. No measurable differences were observed except those attributable to thickness. This method is not sensitive enough to detect a gold atom out of  $\approx 5 \times 10^5$  silicon atoms.

#### 1.1.2.4 Comparisons of Channeling Radiation Between Diamond Structure Crystals

Comparisons between the channeling radiation transition energies from diamond, Si, and Ge are presented in Tables 1-4 and 1-5 (for positrons and for electrons, respectively). For positrons, the photon energy was calculated both from the Doyle-Turner coefficients, based upon the Hartree-Fock model, and from the Moliere potential, based upon the Thomas-Fermi model. [4] Equally accurate results are obtained with the two procedures. For electrons, the photon energies were calculated only from the Doyle-Turner coefficients. Although the agreement with the data for diamond and for Si is fine, the fact that the transition peaks are not resolved individually in the Ge data precluded a detailed comparison with the calculated values.

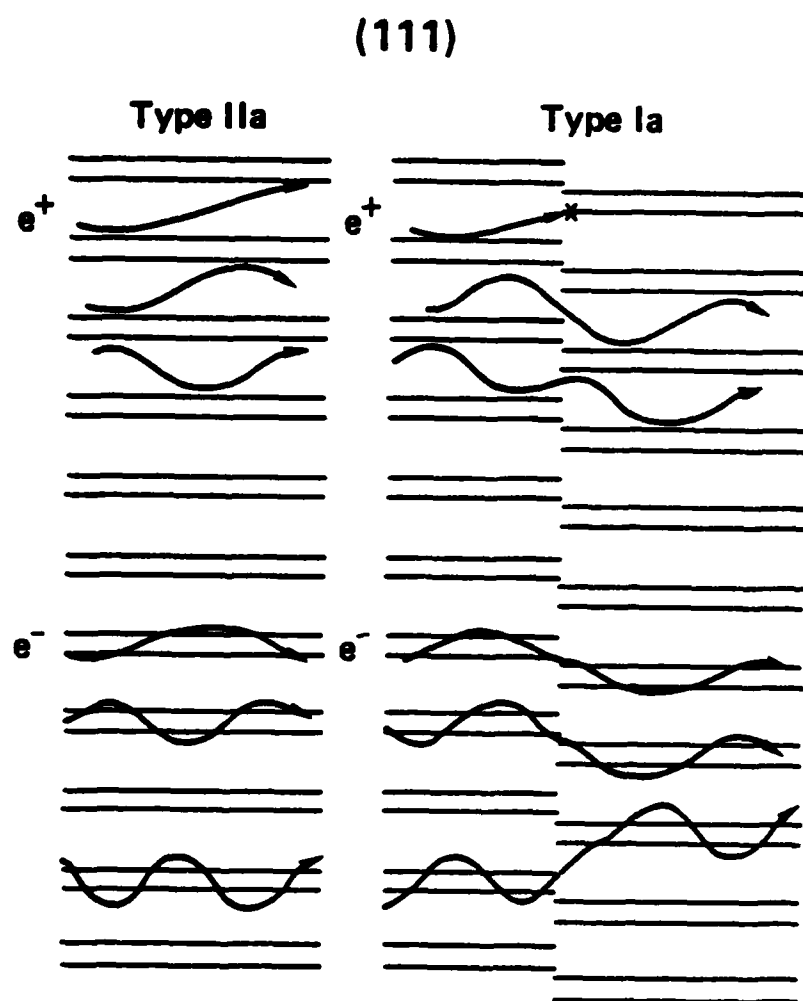


Figure 1-5: Phenomenological semiclassical interpretation of the channeling of positrons and electrons along the (111) planar direction in Type-IIa and Type-Ia diamonds.

Table 1-2: Measured Characteristics of Positron Channeling Radiation from Diamond Crystals.<sup>a</sup>

Plane	Type IIa			Type Ia		
	Peak energy (keV)	Relative intensity	Width (keV)	Peak energy (keV)	Relative intensity	Width (keV)
(111)	54.5 ± 0.3	0.74 ± 0.03	14.1 ± 0.3	53.7 ± 0.3	0.43 ± 0.02	8.9 ± 0.3
(110)	65.3 ± 0.3	1.00	12.0 ± 0.4	63.2 ± 0.4	0.24 ± 0.02	11.4 ± 0.6
(100)	66.6 ± 0.8	0.32 ± 0.03	17 ± 1	67 ± 4	0.04 ± 0.02	20 ± 6

<sup>a</sup>For a positron energy of 54.4 MeV ( $\gamma = 107.4$ ).

**Table 1-3: Measured Characteristics of Electron Channeling Radiation from Diamond Crystals**

Plane	Transition	Type IIa			Type Ia		
		Peak energy (keV)	Relative intensity	Width (keV)	Peak energy (keV)	Relative intensity	Width (keV)
(111) <sup>a</sup>	Several	57.5 ± 1.2	1.44 ± 0.07	24 ± 2	57.3 ± 0.9	1.30 ± 0.05	24 ± 2
(110) <sup>a</sup>	1 → 0	161.9 ± 0.7	0.81 ± 0.04	20 ± 1	No discernible line radiation		
	2 → 1	104.1 ± 0.6	0.58 ± 0.05	19 ± 1			
	3 → 2	77.8 ± 0.4	0.38 ± 0.05	18 ± 1			
	4 → 3	~59	~0.09	~14			
(100) <sup>b</sup>	1 → 0	120.4 ± 0.6	1.00	17.2 ± 0.9	111 ± 2	0.41 ± 0.06	26 ± 3
	2 → 1	65 ± 2	0.16 ± 0.04	17 ± 3	~63	~0.06	~21

<sup>a</sup> For an electron energy of 54.5 MeV ( $\gamma = 107.6$ ).

<sup>b</sup> For an electron energy of 54.2 MeV ( $\gamma = 107.15$ ) for the Type-Ia diamond (only).

**Table 1-4: Characteristics of (110) planar channeling radiation for 54.4-MeV ( $\gamma = 107.4$ ) positrons.**

Crystal	Measured peak energy(keV)	Calculated peak energy (keV)		Measured linewidth (FWHM) (keV)
		Doyle-Turner	Moliere	
Diamond	$65.3 \pm 0.3$	68.5	63.1	$12.0 \pm 0.4$
Silicon	$38.8 \pm 0.3$	41.6	41.3	$9.5 \pm 0.3$
Germanium	$48.1 \pm 0.8$	52.2	51.6	$18 \pm 2$

**Table 1-5: Characteristics of (110) planar channeling radiation for electrons**

Crystal	Transition	Measured peak energy (keV)	Calculated peak energy (Doyle-Turner) (keV)
Diamond <sup>a</sup>	1 $\rightarrow$ 0	$161.9 \pm 0.7$	163.8
	2 $\rightarrow$ 1	$104.1 \pm 0.6$	108.3
	3 $\rightarrow$ 2	$77.8 \pm 0.4$	79.0
	4 $\rightarrow$ 3	$\sim 59$	60.4
Silicon <sup>a</sup>	1 $\rightarrow$ 0	$122.3 \pm 1.0$	122.4
	2 $\rightarrow$ 1	$88.4 \pm 0.5$	88.9
	3 $\rightarrow$ 2	$64.2 \pm 0.5$	64.7
	4 $\rightarrow$ 3	$49.1 \pm 0.6$	49.4
	5 $\rightarrow$ 4	$38.1 \pm 0.3$	38.4
	6 $\rightarrow$ 5	$31.6 \pm 0.3$	$\sim 29$
Germanium <sup>b</sup>	1 $\rightarrow$ 0	Distinct spectral peaks could not be resolved.	176.8
	2 $\rightarrow$ 1		138.7
	3 $\rightarrow$ 2		105.1
	4 $\rightarrow$ 3	The spectral distribution (FWHM) extends from 25 to 190 keV.	78.8
	5 $\rightarrow$ 4		59.3
	6 $\rightarrow$ 5		44.4
	7 $\rightarrow$ 6		32.8

Notes: a.  $E_{e^-} = 54.5$  MeV ( $\gamma = 107.6$ )

b.  $E_{e^-} = 54.2$  MeV ( $\gamma = 107.1$ )

The measured linewidths for positron channeling radiation also are given in Table 1-4. The linewidth for Ge clearly exceeds that for diamond or for Si because the potential anharmonicity is the greatest.

Finally, it is seen (from the tables) that of the three diamond-structure crystals measured, the corresponding channeling-radiation lines for both positrons and electrons are lowest in energy for Si. This shows that the radiation frequency does not depend simply upon atomic number; rather, the lattice dimensions, the atomic radii, and the thermal vibration amplitudes also must be taken into account.

### 1.1.3 Summary of Results

We measured the electron channeling radiation from LiF crystals. These results were compared to the theoretical results calculated from tabulated and empirically-derived vibrational radii. Electron and positron channeling radiation were measured and compared in diamonds with and without platelet defects. The results show very interesting differences. We also measured and compared channeling radiation in silicon with and without gold doping. No measurable differences were observed. Comparisons were made between the channeling radiation transition energies from diamond, Si and Ge and, as expected, there is no simple dependence upon atomic number.

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### 1.1.5 Recent Publications

#### Journal Articles:

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Electron and Positron Planar Channeling Radiation from Diamond.  
accepted by Phys. Lett. A, 1983.
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Characteristics and Applications of Radiation from Channeled Particles.  
to be published in IEEE Trans. Nucl. Sci., Dec 1983.
- [3] Park, H., Swent, R.L., Kephart, J.O., Pantell, R.H., Berman, B.L., Datz, S., and Fearick, R.W.  
Positron and Electron Planar Channeling Radiation from Germanium.  
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Comparison of Channeling Radiation from Diamonds with and without Platelets.  
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- [5] Swent, R.L., Pantell, R.H., Park, H., Kephart, J.O., Klein, R.K., Datz, S., Fearick, R.W., and Berman, B.L.  
Planar and Axial Channeling Radiation from Relativistic Electrons in LiF.  
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**Dissertations: [1]**

- [1] Swent, R.L.  
*Channeling Radiation from Positrons and Electrons.*  
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## 1.2 PHYSICS AND TECHNOLOGY OF SUBMICRON DEVICES

*Principal Investigators:* C.R. Helms, R.F.W. Pease, J.D. Plummer, W.E. Spicer, R.M. Swanson

### Introduction

This research program is divided into a number of projects which are described separately below, including progress in each area during the past year and an outline of future plans. The first three, which report research under the direction of J.D. Plummer, are closely connected in that they are aimed at submicron VLSI devices.

In any MOS or bipolar integrated circuit, there are three generic types of structures. The first is the active switching/amplifying device. We are investigating the characteristics of alternative gate dielectrics for submicron NMOS and CMOS circuits, and thermally grown  $\text{Si}_3\text{N}_4$  and  $\text{SiO}_2/\text{Si}_3\text{N}_4$  composites appear to have significant advantages over  $\text{SiO}_2$ . This first project is aimed at evaluating material properties and corresponding device characteristics associated with this alternative dielectric.

The second generic type is a parasitic device and is the result of the local-oxidation techniques commonly used for device-to-device isolation. Such isolation is generally achieved in both bipolar and MOS integrated circuits through selective field oxidation coupled with self-aligned ion-implanted channel stops. Despite its current technological dominance, this isolation technique will be inadequate as device geometries approach  $1\text{ }\mu\text{m}$  and, ultimately, submicron sizes. As a result, the scientific objectives of this second project are to:

1. use two-dimensional numerical simulation to determine and better understand the limits of local-oxidation device-isolation schemes and
2. investigate, both theoretically and experimentally, isolation techniques that may improve the isolation characteristics at feature sizes of  $\leq 1\text{ }\mu\text{m}$ .

The third generic type is generally a passive load element which, in bipolar circuits, often takes the form of diffused or ion-implanted resistors. In NMOS circuits, the most common device is a polysilicon resistor. Polysilicon layers are also widely used as gate electrodes and for interconnections in MOS circuits. In this third project, we are investigating the limiting behavior of polycrystalline silicon layers when they are defined with lateral and vertical dimensions comparable to the grain sizes in the material. Because grain sizes are typically  $0.1$  to  $0.5\text{ }\mu\text{m}$  following high-temperature processes, the dimensions of interest are on the same order as the NMOS channel lengths in the first two projects described above. We plan to analyze in detail the material and electrical properties of a single grain boundary in polysilicon. All current models of polysilicon

properties rely on the statistically averaged behavior of many grain boundaries in series; however, in small-geometry structures, this will not be a reasonable assumption.

In summary, we are engaged in a coherent investigation of the problems of submicron silicon integrated circuits, and the three projects are aimed at the three key components of any modern silicon circuit. Our intent is to establish a scientific basis for understanding and circumventing problems that may occur in scaling the three generic structures to submicron dimensions.

### 1.2.1 ALTERNATIVE GATE DIELECTRICS FOR SUBMICRON MOS VLSI

*Investigators:* M.M. Moslehi, K.C. Saraswat, J.D. Plummer

#### 1.2.1.1 Scientific Objectives

High quality, very thin (<100 angstrom) gate insulators (VTGI) will be required for future scaled VLSI devices. To illustrate the trend of the larger scale of integration and the need for thinner gate insulators, DRAM can be used as an example. The 256 Kbit DRAM has a gate insulator thickness of about 200 angstrom whereas the projected 1 Mbit DRAM using a conventional one transistor cell per bit will require an insulator thickness of less than 100 angstrom.

Some of the reasons and motivations for using thinner gate insulators are:

1. They reduce the undesired second order device effects such as short-channel and narrow-channel effects and subthreshold conductivity in weak inversion region [6].
2. They allow an increase in integration density and improved speed-power product as suggested by scaling laws. [2]
3. In very thin gate insulators the effects of fixed insulator charges and mobile ions on threshold voltage are insignificant [6].
4. Very thin gate insulators thinner than those expected by scaling laws, improve the device characteristics and can reduce alpha particle disturbances because of a larger transconductance and a higher density of carriers induced in the channel.

VTGI should be grown using an easily controllable process with a minimum number of process control parameters. They should be uniform and amorphous with a low defect density and conductivity. Furthermore, high breakdown field, sharp breakdown distribution, a clean interface, and low trapping efficiency are important requirements. In order to have better control over electrical characteristics of devices, VTGI should be effective masks against impurity diffusion.

The yield and reliability of silicon dioxide films in the very thin regime (<100 angstrom) is

questionable [11]. The process control to grow these films reproducibly is difficult. Very thin  $\text{SiO}_2$  layers are not a good mask against impurity diffusion [3, 9] and they have a high defect density [10]. These poor properties of very thin  $\text{SiO}_2$  films and also their tendency to react with electrode materials will limit their effective widespread application for gate dielectrics of scaled VLSI devices.

Thermally grown very thin films of silicon nitride have a number of advantages over silicon dioxide. Their growth is self-limiting and therefore easily controllable. They have fewer process control parameters and high oxidation resistance. Moreover, they are effective barriers against impurity diffusion and their characteristics do not degrade during VLSI processes [12, 7]. Devices fabricated with these films show a large transconductance and reduced undesired second order effects [6, 8, 5].

Conventionally, thermal nitridation of silicon has been done in resistance-heated hot-wall quartz-tube furnaces which can lead to high oxygen contamination of the grown films. In the work reported here, thermal nitridation was accomplished in a closed-tube cold-wall rf-heated reactor. The grown films have been characterized using grazing angle RBS, AES, ellipsometry, and etch rate measurements. In addition, the electrical properties of the films were determined by C-V and I-V measurements on Al-gate capacitors.

#### 1.2.1.2 Progress

All experiments were conducted in a horizontal rf-heated reactor operating at atmospheric pressure as shown in Figure 1-6. Thermal nitridation is performed in pure ammonia or diluted ammonia in argon. The oxygen contamination from outside and from the quartz tube is insignificant.

Both n- and p-type, (111) and (100) silicon wafers with resistivities ranging from 0.002 to 3 ohm.cm, and oxidized silicon wafers (oxide thickness = 95 angstrom) were used. The samples were first cleaned chemically, loaded on a silicon carbide-coated graphite susceptor and then inserted in the quartz tube. After an initial purging of the system with pure nitrogen, the flow of pure ammonia (<1 ppm contaminants) was established. After flushing  $\text{N}_2$  out of the tube with ammonia, the temperature was ramped up to the growth temperature and stabilized. Nitridations were performed at temperatures ranging from 950°C to 1230°C for periods of 30 minutes, 1 hour, 2 hours, and 4 hours.

For the nitridation of  $\text{SiO}_2$ , 95 angstrom of silicon dioxide was grown thermally at 900°C for 20 minutes in dry oxygen and was annealed in argon at the same temperature for 90 minutes to minimize the fixed oxide charge.

The thicknesses of the grown thermal silicon nitride films were measured using a microcomputer-

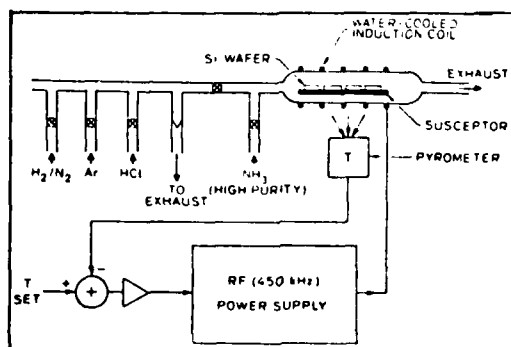


Figure 1-6: Thermal nitridation reactor

controlled ellipsometer with a 6328 angstrom laser source and substrate index of refraction fixed at  $3.85 - i0.02$ . In the measurements the refractive index of the silicon nitride films was fixed at 2.0, 1.3 and 1.6. This method is adopted because it is not possible to measure both thickness and refractive index of very thin films ( $<100$  angstrom) accurately by ellipsometry. The variation of the film refractive index in the range between 1.6 and 2.0 exhibits little effect on the nitride thickness measurement results. The measured thickness values are almost independent of the film refractive index  $N_f$  for values in between 1.8 and 2.0. However, all kinetic data presented in this report are for  $N_f = 2.0$  which is the established value for thick CVD nitride.

To investigate the effect of heavy doping, an experiment was performed where heavily phosphorous doped silicon wafers with (100) and (111) orientations were nitrided at  $1190^\circ\text{C}$  for 2 hours. Phosphorous doping was previously done at  $1050^\circ\text{C}$  from  $\text{POCl}_3$  resulting in a sheet resistance of 1.6 ohms/square.

To fabricate MNS and MOS capacitors, aluminum was evaporated using flash evaporation on the frontside with nitride and nitroxide gate insulators and on the backside after etching the backside insulator films. The wafers were then annealed in forming gas at  $450^\circ\text{C}$  for 20 minutes. Finally aluminum was patterned into dots with diameters ranging from 100 to  $1600\ \mu\text{m}$ .

*1. Growth Kinetics:* Figure 1-7 shows the thickness of the thermal silicon nitride films as a function of

nitridation temperature for nitridation periods of 30 minutes, 1 hour, 2 hours, and 4 hours on (100) and (111) silicon wafers. Under identical processing conditions the films grown on (100) silicon are thinner than those on (111) silicon, and the effect is stronger at higher temperatures. However, below 1000°C the effect of the substrate orientation on nitridation kinetics is negligible. It is evident that in contrast to the silicon thermal oxidation process, the nitridation kinetics have a rather weak dependence on the substrate orientation. This could be due to the fact that the latter process is diffusion-limited except for the fast initial growth.

For shorter times, nitridation of silicon varies with temperature, approximately according to an Arrhenius plot (See Fig. 1-7 for  $t = 30$  minutes) whereas for longer times ( $t > 1$  hour) the behavior is non-Arrhenius. Applying exponential least-squares curve fits of the form  $X_N = X_\infty \text{EXP}(-E_a/kT)$  to the experimental results of Figure 1-7 the values of the activation energy  $E_a$  and the coefficient  $X_\infty$  (the thickness as  $T \rightarrow \infty$ ) were evaluated as a function of time with orientation as a parameter. Nitridation of (111) silicon shows a higher activation energy than that of (100) silicon. The activation energies as given in Table 1-6 are fairly small but larger than those reported by Murarka et al [12].

Thermal nitridation of silicon dioxide resulted in an increase in the film thickness. Oxide films of 95 angstrom thick were thermally nitrided at various temperatures for periods of 30 minutes, 1, 2, and 4 hours. The thickness increase as a function of processing temperature and time is shown in Figure 1-8. It does not show an Arrhenius behavior with temperature because the film thickness increases more rapidly at higher temperatures. The thickness of all nitrided oxide films were measured using an ellipsometer with the film optical refractive index at 1.46. However, the oxide samples nitrided at very high temperatures for long periods (e.g. 1200°C, 4 hours) exhibited enhanced refractive indices up to more than 1.7. Our experience shows that in the thickness measurement of very thin films by ellipsometry, fixing the refractive index at a value lower than the true index value, results in a measured value slightly higher than the real thickness. Therefore, in the foregoing high temperature experiments for long processing times the measured thickness might be somewhat higher than the actual value.

To express the experimental kinetics results in a functional form, we have found the following simple empirical relationships useful:

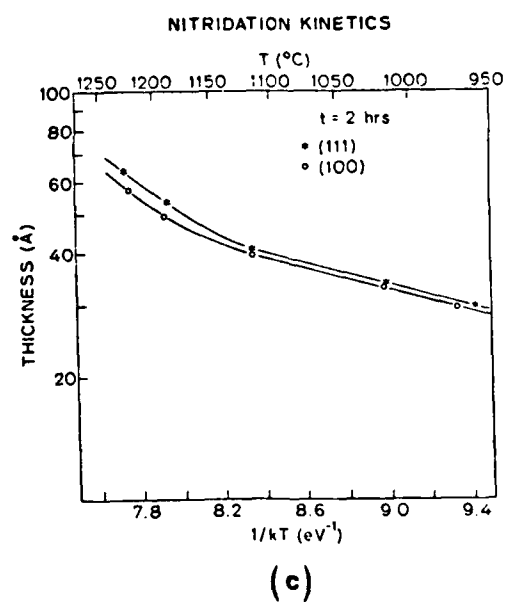
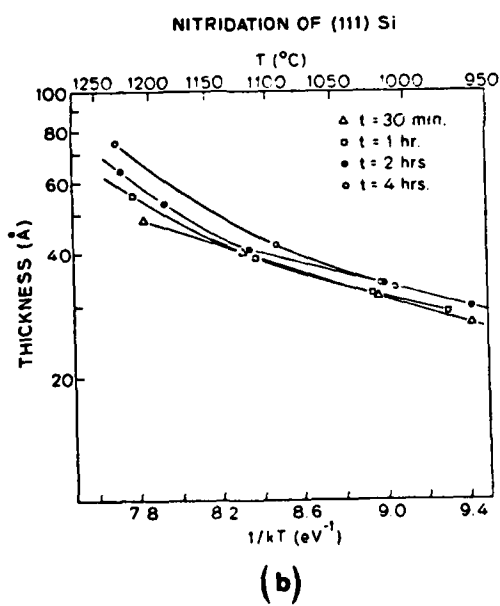
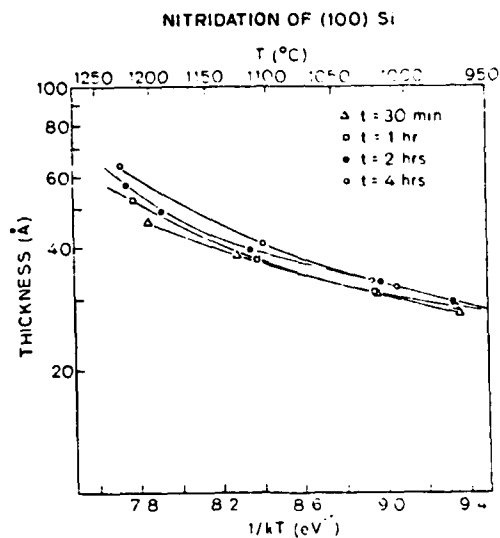
$$X_N = a \times \ln(1 + b\sqrt{t}) \quad (1.1)$$

$$X_N = a \times \exp(-b/\sqrt{t}) \quad (1.2)$$

$$X_N = \ln(1 + a \times t^b) \quad (1.3)$$

$$X_N = a \times \ln(1 + b \times t) \quad (1.4)$$

$$X_N = a \times t^b \quad (1.5)$$



**Figure 1-7: Dependence of thermal nitride thickness on nitridation time and temperature.**

(a) on (100) silicon, (b) on (111) silicon, (c) Growth kinetics on (100) and (111) silicon for  $t = 2$  hours.

Table 1-6: Activation Energies

Nitridation Time	(100)		(111)	
	X(angstrom)	E <sub>a</sub> (eV)	X(angstrom)	E <sub>a</sub> (eV)
30 min	667.4	0.342	869.5	0.369
1 hour	1052.9	0.390	1525.2	0.429
2 hours	1183.9	0.398	1706.0	0.434
4 hours	3295.1	0.513	7455.2	0.602

The constants  $X_{\infty}$  and  $E_a$  ( $X_N = X_{\infty} \text{EXP}(-E_a/kT)$ )  
for various nitridation times of (100) and (111) silicon

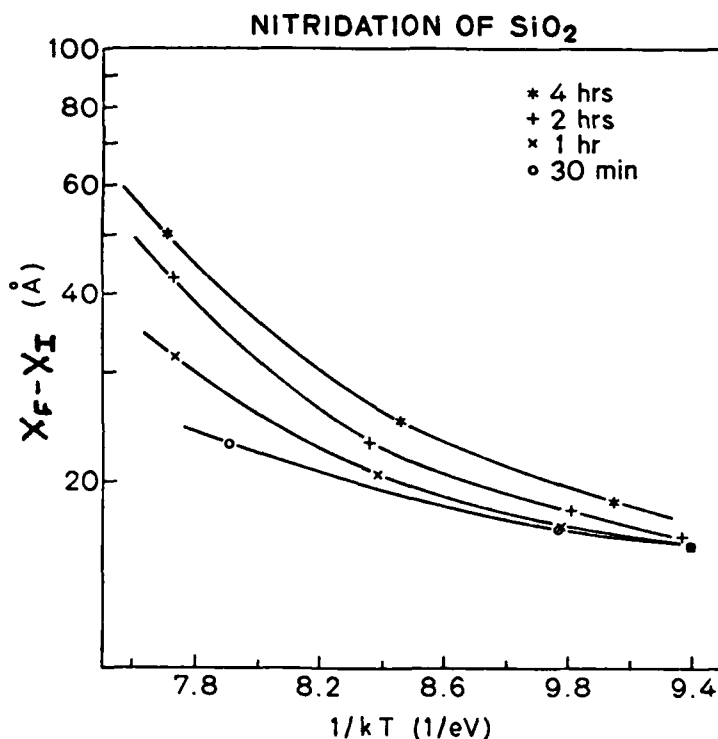
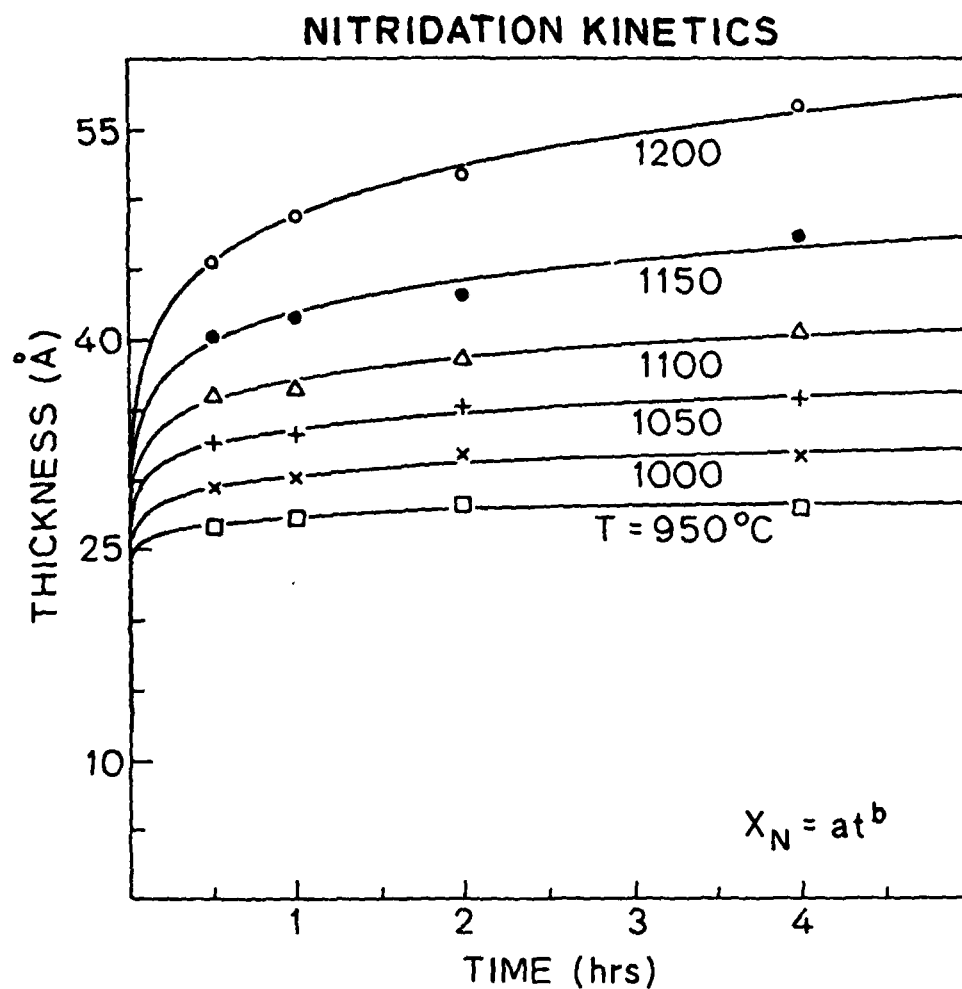


Figure 1-8: Thickness increase of 95 angstrom silicon dioxide due to thermal nitridation as a function of nitridation time and temperature

where  $a$  and  $b$  are temperature dependent constants and  $X_N$  and  $t$  are the silicon nitride thickness and nitridation time, respectively. In these relationships the constants  $a$  and  $b$  are found by fitting the experimental data using the method of least-squares. Figure 1-9 shows an example in which our results and also experimental data from reference [1] were fitted to Eq. (1.5).





**Figure 1-9:** Experimental thermal nitride growth kinetics data which were fitted to Equation (1.5) as shown by the solid curves.

In the experiments conducted to study the effects of heavy doping on nitridation kinetics, we observed that under identical processing conditions, the nitride films grown on heavily phosphorous doped silicon had the same thickness as those grown on lightly doped silicon wafers. Therefore, no significant effect on heavy doping on nitridation growth kinetics was detected.

*II. Auger electron spectroscopy:* Some of the nitride and nitroxide samples were analyzed using AES (4500 eV primary electron source). AES depth profiles for several silicon nitride and nitroxide samples are shown in Figure 1-10. The results indicate that the nitrogen concentration decreases

smoothly from the surface towards the interface. In Figure 1-10 all the nitrogen intensity profiles should be multiplied by 1.9 for direct comparison with oxygen intensity profiles. In thermal nitride samples, the oxygen concentration builds up towards the surface of the film and its maximum is at the surface. This behavior can be explained as follows. At the beginning, the nitridation process is reaction-limited and proceeds easily until it is limited by diffusion which significantly slows down the process. At this point, nitridation mainly occurs closer to the surface region and inside the film based on our AES analysis results. This process consumes the excess silicon inside the film and is the reason for the higher oxidation resistance of the films nitrided for longer periods in contrast to those nitrided for shorter periods at the same temperature. Subsequently, residual oxidant impurities in the nitridation ambient partially oxidize the surface of the nitride film which contributes to the oxygen concentration peak at the surface. In addition, the initial native oxide on the surface of cleaned silicon wafers also contributes to the oxygen concentration of the films. According to Figure 1-10 the nitrogen concentration profile in thermal nitride films has a peak very close to the surface region (but not at the surface) and then decreases towards the interface. The film grown at 1105°C for 4 hours shows an average relative atomic nitrogen concentration of more than 85% as calculated from AES data in Figure 1-10(c). The relative nitrogen atomic concentration ( $[N]/([N] + [O])$ ) is defined as the nitrogen concentration divided by the total nitrogen and oxygen concentrations. This is about 25% purer than the best films grown in hot-wall resistance-heated furnace system by Murarka et al [12] and those fabricated in a closed-tube hot-wall system by Hayafuji and Kajiwara [4]. To achieve reproducible growth results and process control and to grow high quality thermal nitride films the level of oxygen contamination should be minimized as was done in this work. Under identical growth conditions, due to oxygen contamination, the films grown in hot-wall furnace systems are thicker than those grown in our reactor. The AES analysis data in Figure 1-10 for thermal nitride films indicate that the silicon concentration increases from the surface towards the interface. The nitride films are found to have a wider transition width (defined as the ratio of transition width to the total thickness) than thicker oxide films.

The relative amount of excess silicon incorporated into the nitride films was found to be higher for the films grown at lower temperatures for shorter times. The results obtained from AES analysis data support the idea that the nitridation reaction does not take place just at a plane surface located at the nitride/silicon interface but also occurs throughout the nonstoichiometric bulk of the film. This is also confirmed by the fact that following the fast initial growth, the thickness increases very slowly, but the nitrogen concentration profile shifts upward to have higher concentration values indicating the existence of bulk as well as surface reaction.

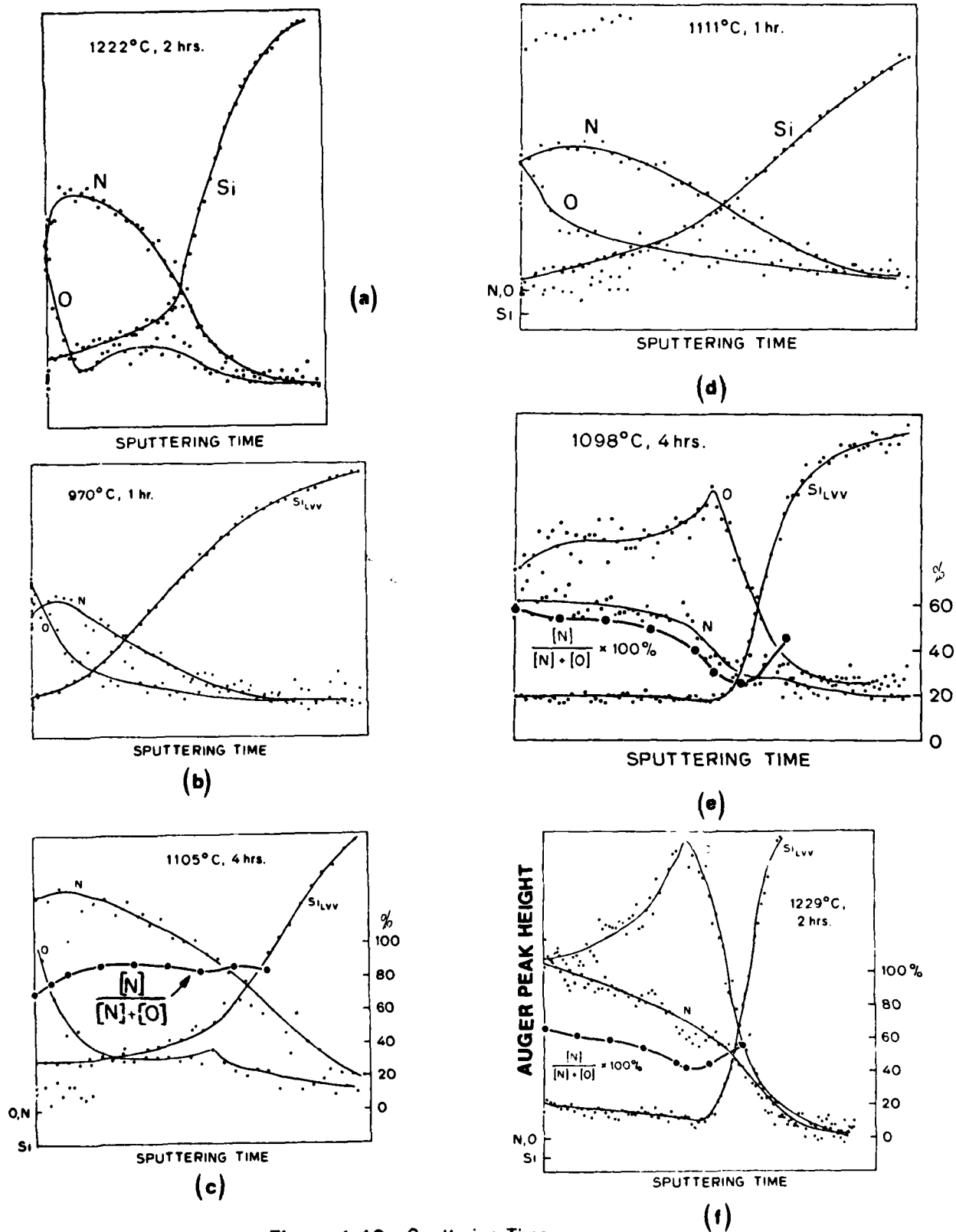


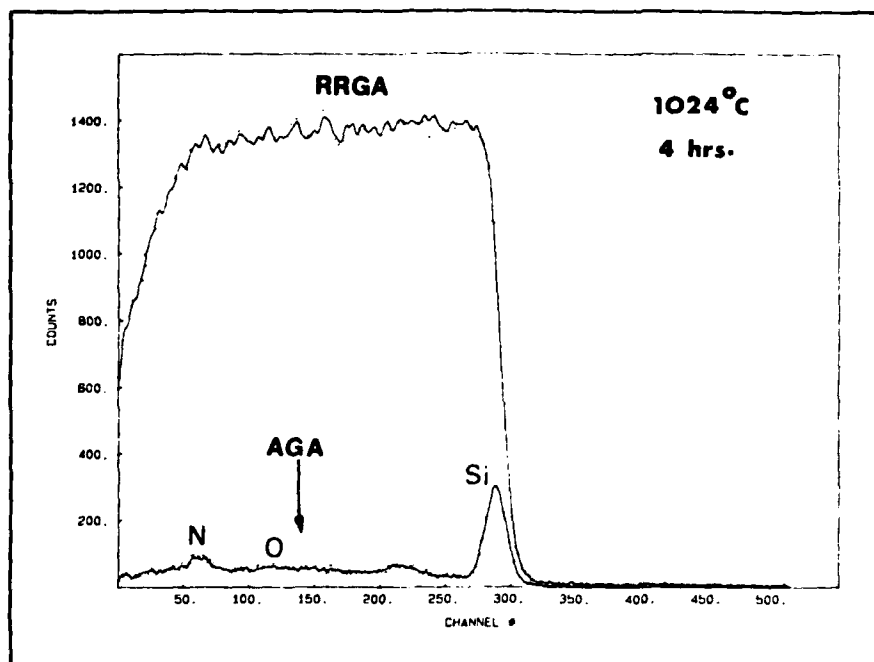
Figure 1-10: Sputtering Time

As shown in Figure 1-10(e), for 95 angstrom oxide samples nitrided at 1098°C for 4 hours the fractional nitrogen concentration is more than 50% at the surface. However, at higher temperatures following some initial nitridation of the surface and interface, the nitridation process mainly proceeds at the surface region. This will also be justified in our later discussion on etch rate measurement results but for now we can explain it using Figure 1-10(c) and 1-10(f). Figure 1-10(e) shows a fairly uniform nitrogen profile which decreases slowly towards the interface whereas Figure 1-10(f) for the sample nitrided at higher temperature indicates a faster decrease of nitrogen concentration towards the interface with a large concentration at the surface. Figure 1-10(e) and Figure 1-10(f) also show that the relative nitrogen concentration in nitrided oxide films decreases slowly from the surface into the bulk of the film, reaching a minimum at a region close to the interface followed by an increase towards the interface. This minimum arises from a peak in the oxygen concentration profile between the surface and the interface which is closer to the interface region. The oxide samples nitrided at lower temperatures show less peak-to-peak variation of oxygen concentration.

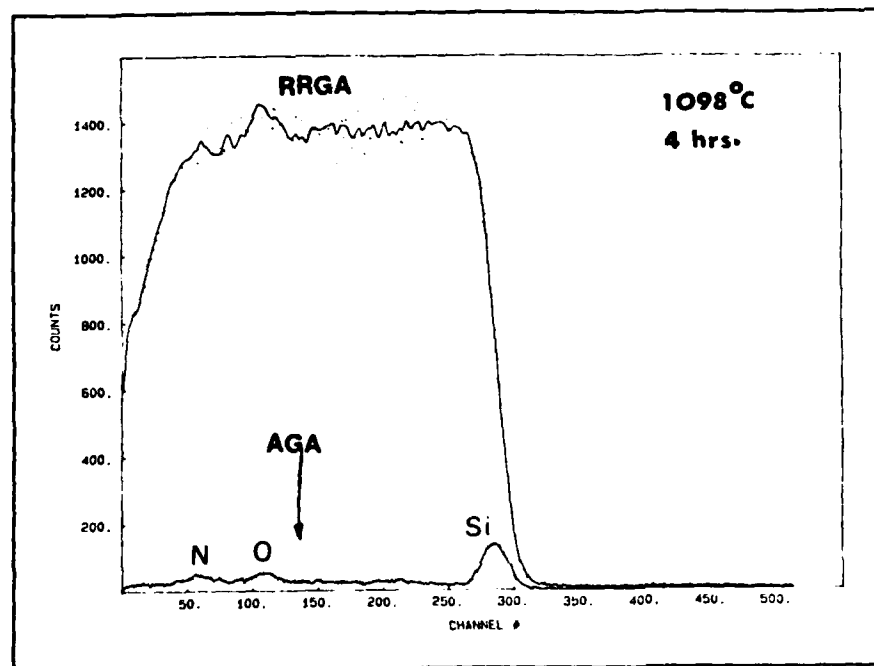
*III. Grazing angle RBS:* Grazing angle Rutherford backscattering is a sensitive and useful technique for the compositional characterization of very thin films due to its enhanced depth resolution. For analysis of our samples, the detector was placed at a grazing angle of 85° with respect to the incident 2.2 MeV helium ion beam. The particles backscattered from the silicon substrate are not collected by the grazing angle detector, resulting in an improved signal to noise ratio for thin film analysis. One may note that in the conventional RBS analysis, the detector is placed at a scattering angle of 170°.

Figure 1-11 shows the results of RBS analysis for a thermal nitride and a nitroxide sample. In these plots, the curves designated by RRGA are for rotational random grazing angle measurements and the curves AGA are obtained using aligned grazing angle technique. In the aligned spectra, the peaks for elements with larger atomic masses occur at higher channel numbers or energies. The aligned grazing angle spectrum for the nitroxide film consists of three peaks for nitrogen, oxygen, and silicon, respectively. The thermal nitride sample shows a much smaller oxygen peak than the nitrided oxide film which is an indication of a low level of oxygen contamination. Chemically cleaned silicon wafers and thin silicon dioxide films were used as reference. The measured areas under the nitrogen, oxygen, and silicon aligned peaks can be used to calculate the atomic concentration ratios of these elements. For instance, the nitrogen to oxygen areal concentration ratio is found using the following equation:

$$\frac{[N]}{[O]} = \left( \frac{A_N}{\sigma_N(E_o)} \right) \times \left( \frac{\sigma_O(E_o)}{A_O} \right) \quad (1.6)$$



(a)



(b)

Figure 1-11: Grazing angle RBS analysis results. (a) Thermal nitride, (b) Nitroxide

where  $A_N$  and  $A_O$  correspond to the nitrogen and oxygen areas and  $E_0$  is the incident helium ion energy. The ratio  $\sigma_O/\sigma_N$  can be approximated by:

$$\frac{\sigma_O}{\sigma_N} = \left( \frac{Z_O}{Z_N} \right)^2 = \left( \frac{64}{49} \right) \quad (1.7)$$

where  $\sigma_O$ ,  $Z_O$ ,  $\sigma_N$ ,  $Z_N$  are oxygen and nitrogen cross sections and atomic numbers, respectively. As a result:

$$\frac{[N]}{[O]} = \left( \frac{A_N}{A_O} \right) \times \left( \frac{Z_O}{Z_N} \right)^2 \quad (1.8)$$

Table 1-7 shows the calculated values for relative oxygen areal density ( $[O]/([O] + [N])$ ) for several silicon nitride and nitroxide samples grown under different processing conditions. These results indicate that most of the silicon nitride films have less than 20% relative areal oxygen concentration which is in good agreement with those values calculated from AES analysis data.

**Table 1-7: Relative oxygen areal density for several silicon nitride and nitroxide samples**

Sample #	Treatment	$\frac{[N]}{[O]}$	$\frac{[O]}{[N] + [O]} \times 100\%$
20-A	1150°C, 2 hr	4.60	% 17.9
19-A	1111°C, 1 hr	4.14	% 19.5
11-A	1204°C, 30 min	4.20	% 19.2
24-B	1024°C, 4 hr	5.71	% 14.9
23-B	1105°C, 4 hr	3.74	% 21.1
23-D	1098°C, 4 hr	1.27	% 44.1

The values of relative oxygen areal density for several silicon nitride and nitroxide samples grown under various nitridation conditions.

*IV. Etch rate measurements:* To further study the film composition as a function of depth, etch rate measurements were performed employing step by step etching of the samples. In these measurements, the film thickness was measured using ellipsometer (The optical refractive index was

fixed at 2.0 and 1.46 for nitride and nitroxide films, respectively.) after each etching step in a 2% by volume solution of HF in water at room temperature. As illustrated in Figure 1-12, the etch characteristics for thermal silicon nitride films show a faster etch rate at the surface followed by a fairly constant etch rate. The faster rate at surface is due to the oxygen concentration peak in this region.

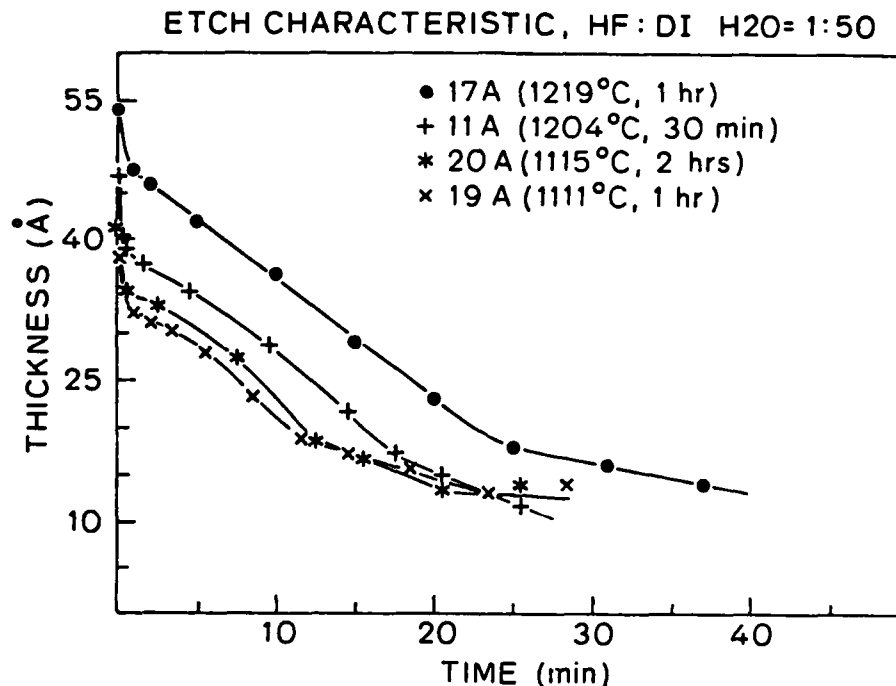


Figure 1-12: Etch characteristics of thermal nitride samples grown under various nitridation conditions

The etch characteristics for two nitroxide samples are shown in Figure 1-13 in which oxide and typical thermal nitride etch characteristics are shown for comparison. The oxide sample nitrided at 115°C for two hours shows three distinct regimes. The surface and interface regions have smaller etch rates than the intermediate region whose etch rate is close to the etch rate for reference oxide (48 angstrom/min). This again confirms the results of AES analysis. The faster etch rate in the intermediate region is caused by the higher oxygen concentration in this region as discussed in the AES analysis section. According to Figure 1-13, for the oxide sample nitrided at 115°C, the surface etch rate (10.6 angstrom/min.) is higher than that close to the interface. On the other hand, the oxide sample nitrided at higher temperature (1227°C, 1 hour) has a slower surface etch rate than the first sample, and very close to that of thermal nitride. Close to the interface, the etch rates in both the nitroxide samples are equal as shown in Figure 1-13. Based on the results of etch rate measurements

we conclude that the initial nitridation of oxide proceeds mainly close to the oxide/silicon interface and surface and then essentially occurs in the region close to the surface. This interpretation is in agreement with the form of AES nitrogen depth profiles of oxide samples nitrided at high temperatures in contrast to those nitrided at lower temperatures as explained before.

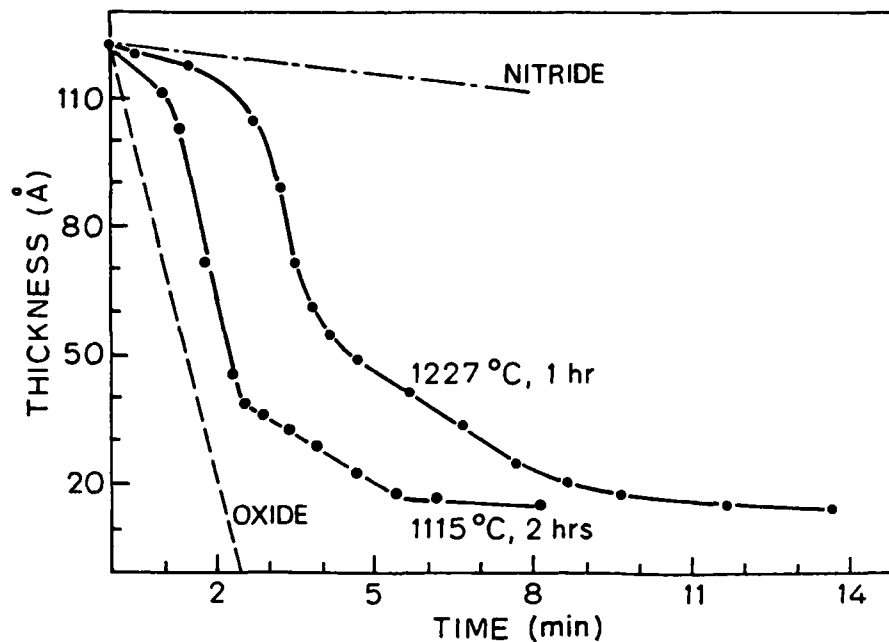
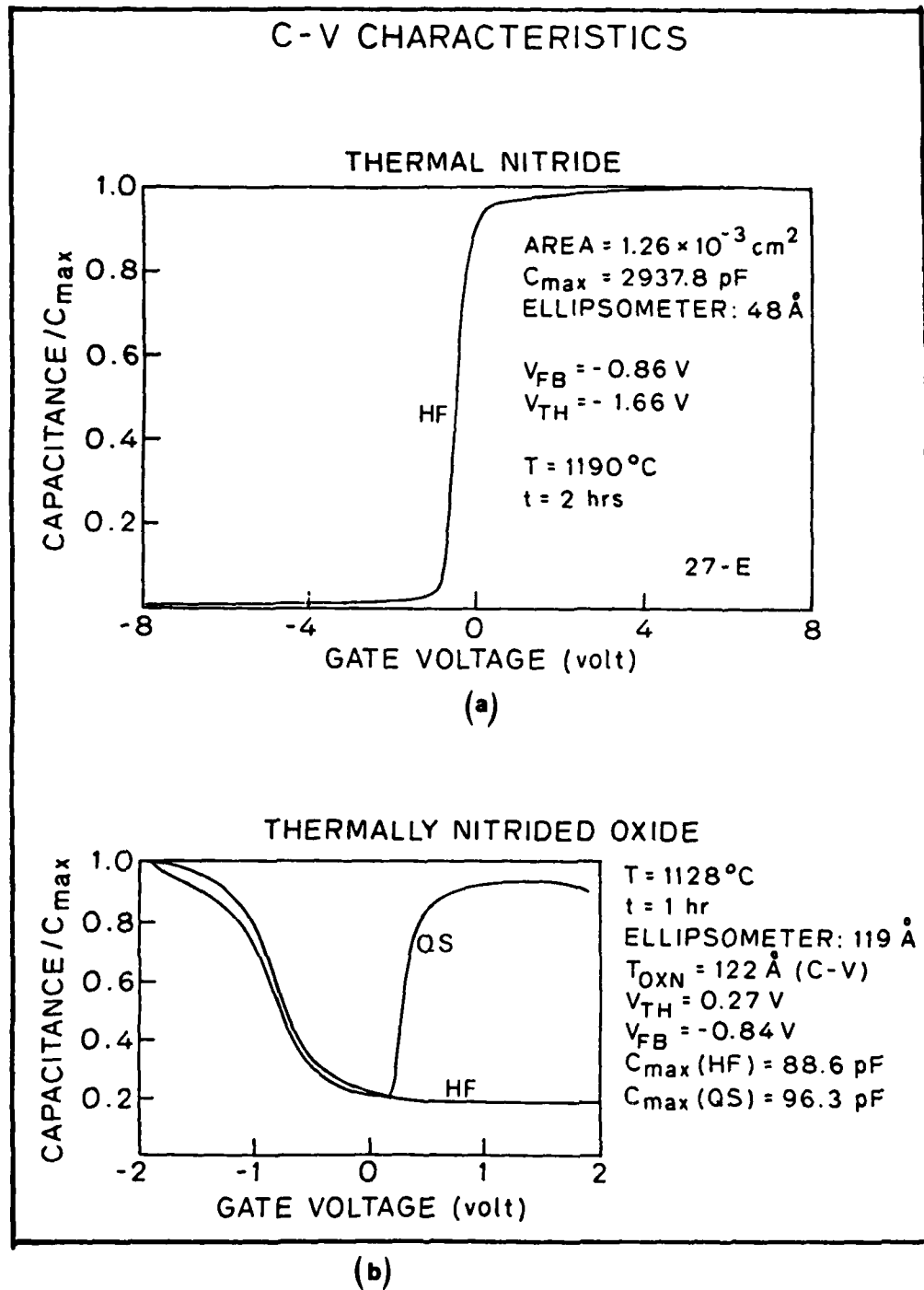


Figure 1-13: Etch characteristics of two nitroxide samples

V. *Electrical characteristics:* Metal-insulator-semiconductor (MIS) capacitors were fabricated using thermal silicon nitride and nitroxide films as gate dielectrics and were electrically tested using C-V, I-V, and breakdown measurement techniques. Figure 1-14(a) illustrates the high frequency (1 MHz) C-V characteristic for a capacitor with thermal nitride insulator on n-type silicon. The high frequency and quasiStatic C-V characteristics for another capacitor with nitroxide insulator on p-type silicon are shown in Figure 1-14(b). The permittivity of the thermal nitride insulator was calculated using the ellipsometry thickness measurement result and the measured capacitance in the accumulation region. The results exhibit a larger value than that reported for CVD nitride [13]. Due to the higher conductivity of very thin thermal nitride compared to the thicker oxide, the conventional quasi-static method is not a useful and accurate technique for devices with thermal nitride films. The reason is that usually the conduction current dominates the capacitive displacement current specially for higher applied voltages. Therefore, an improved technique is being developed to overcome this problem.





**Figure 1-14:** C-V characteristics of MIS structures using (a) thermal nitride and (b) nitroxide gate insulators

Figure 1-15 shows the conduction characteristic (I-V) for a thermal nitride film used in an MIS

structure. The conduction in thin films of thermal nitride is expected to be dominated by the Fowler-Nordheim tunneling mechanism, especially for large electric fields. The tunnel emission is either caused by field ionization of trapped electrons into the conduction band of the thermal nitride or electrons which tunnel from gate electrode into the conduction band of thermal nitride. Among the basic conduction processes in insulators, the tunnel emission has the strongest dependence on the applied voltage and is expressed as:

$$J = a \cdot V^2 \cdot \exp(-b/V) \quad (1.9)$$

where  $J$  and  $V$  are the current density and applied voltage, respectively. The constants  $a$  and  $b$  are temperature-independent. When the dominant conduction mechanism in thermal nitride films is tunneling, a plot of  $\log(J/V^2)$  versus  $1/V$  should generate a linear straight curve. Figure 1-16 shows this type of plot for the conduction data in Figure 1-15. It is a linear curve for high fields which corresponds to conduction by tunneling. For lower field the behavior is different which can be attributed to the contribution of other conduction mechanisms and also to the fact that for small voltages the capacitor is not completely in the accumulation region.

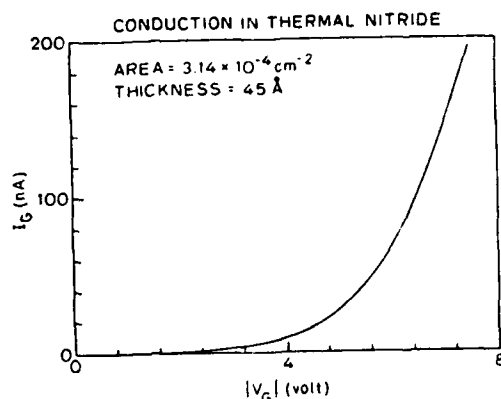


Figure 1-15: The conduction characteristic of a thermal nitride gate insulator

Experiments with ultrathin thermal nitride films exhibited very large breakdown fields on the order of 20 MV/cm which is higher than the values for oxide and thick CVD nitride. Figure 1-17 shows a worst case breakdown characteristic for a 45 angstrom thermal nitride gate insulator used in an Al-gate capacitor. An Al-gate device using 119 angstrom nitroxide showed a typical breakdown field on the order of 10 MV/cm which is half of that observed for thermal nitride.

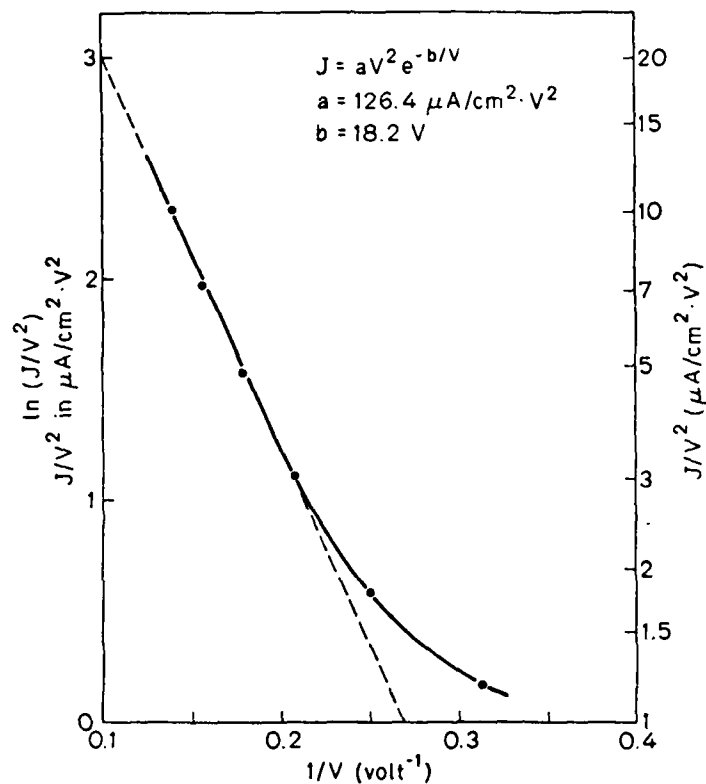


Figure 1-16:  $J/V^2$  versus  $1/V$  for a thermal nitride gate insulator using the conduction data in Figure 1-17

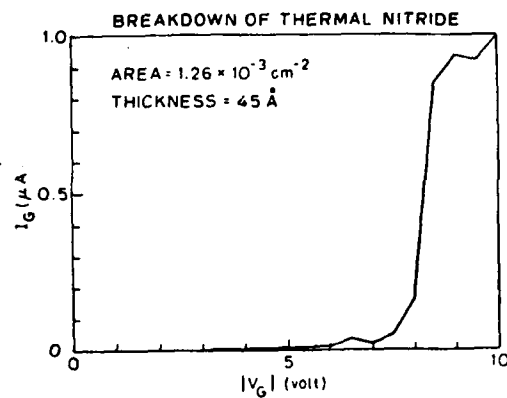


Figure 1-17: Breakdown characteristic of a thermal nitride gate insulator

### 1.2.1.3 Summary of Results

Very thin silicon nitride and nitroxide films were thermally grown in a cold-wall rf-heated reactor. Growth kinetics of these processes and the effects of heavy doping have been investigated. Composition of the films grown under different processing conditions have been analyzed by AES, grazing angle RBS, and etch rate measurements. In addition, the films were electrically characterized using C-V, I-V, and breakdown techniques. The results of this study show that thermally grown, very thin silicon nitride and nitroxide films will be very good gate insulators for future scaled-down VLSI devices.

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Electrical Characteristics of Devices Fabricated with Ultrathin Thermally Grown Silicon Nitride and Nitroxide Gate Insulators.  
To be presented at the 1983 Symposium on VLSI Technology, Maui, September 1983.

### 1.2.2 ISOLATION TECHNIQUES SUITABLE FOR SUBMICRON TECHNOLOGIES

Investigators: S. Goodwin, J. Plummer

#### 1.2.2.1 Scientific Objectives

In N-channel MOS technology, device isolation is almost universally achieved by ion-implantation doping of the field region followed by local oxidation to form a thick field oxide (LOCOS). The active device regions are protected from these steps by a masking layer of silicon nitride which is subsequently removed. This technique, illustrated in Figure 1-18, has the following advantages:

- The field oxide is self-aligned to the more heavily doped channel region.
- The ion implantation protects against field surface inversion and allows an optimum choice of substrate doping for the active devices.
- Overall packing density increases by using the field oxide as a portion of the source/drain mask.
- Because local oxidation consumes silicon, the step height difference between the field and device regions is reduced.

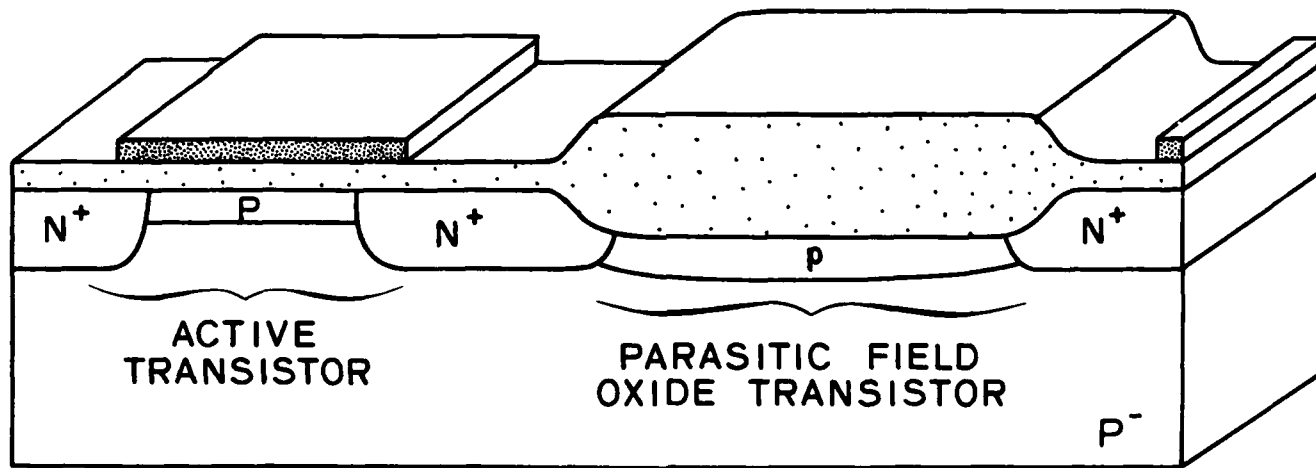


Figure 1-18: Cross-section of a chip showing an active transistor, and a parasitic field oxide transistor

Figure 1-18 shows the cross-section of a chip, showing an active transistor, and a parasitic field

oxide transistor. The parasitic transistor is between the active transistor on the left, and another, partially drawn, on the far right. The relatively thick oxide and high substrate (P implant) doping levels produce relatively poor subthreshold slopes in the parasitic device so that device-to-device isolation is best characterized by the leakage (subthreshold) current that flows for a given gate voltage.

The principle disadvantage is the chip area consumed. Because of the lateral diffusion of the channel stop and the lateral oxidation (bird's beaking), the electrical length of the channel stop region is significantly larger than the mask dimensions. As active device dimensions continue to shrink, the field regions take an increasingly disproportionate amount of surface area due to the difficulty of scaling the LOCOS structure.

The objective of this project is to investigate device isolation techniques that would best resolve this problem, by understanding the device physics of isolation structures. There are two principle thrusts in the investigation. One is to examine the limits of the present technology as it is scaled down. The other is to analyze alternative isolation techniques to determine their limits in comparison to today's technology, including some techniques recently suggested in the literature [5, 4, 1].

#### 1.2.2.2 Progress

Extensive work on these problems has been done with a two dimensional device simulation computer program, GEMINI, written by J.A. Greenfield of the Stanford Integrated Circuits Laboratory [3]. These simulations showed that the use of trench-like isolation structures significantly improves device electrical isolation, provided junction depths are less than the trench depth.

To understand this effect, consider the structure of Figure 1-19. If the source/drain junctions are shallow so that they lie above the oxide/semiconductor interface, or if the isolation oxide is produced in an etched trench, then the conduction channel extends around the oxide corners. The device physics then become two dimensional in nature as can be seen in the plot of the surface potential. Instead of the potential barrier being centered under the gate, it is now located at the oxide corners. This can be understood by examining a region bounded by the oxide/semiconductor interface, the depletion edge, and two electric field lines. At the planar region in the middle of the channel, this region is rectangular in shape, while the analogous region at the corner of the oxide is pie-shaped. Thus for equal interface areas and depletion widths, the pie-shaped region will contain more bound depletion charge than is needed to support the gate voltage; therefore, the depletion width is less at the corner than at the middle of the channel. Because the depletion width is smaller, there is less band bending and hence the potential at the corner is less as well. This results in the potential distribution shown. As the gate voltage increases from a low value, the potential at the corners increases much more slowly than in the middle of the channel.

In Figure 1-19, the source/drain junctions have been pulled up to expose the corners of the oxide. The gate is biased for  $1\text{pA}/\mu\text{m}$ . The potential barriers are now at the corners of the oxide.  $V_s = 0$ ,  $V_d = 0$ ,  $V_{\text{sub}} = 0$ ,  $V_g = 18$ ,  $N_a = 2 \times 10^{16} \text{ cm}^{-3}$ . Simple 1D MOS theory predicts the potential barrier height in the center region of the device (planar device). 2D effects due to charge sharing in the corner regions produce a substantially larger potential barrier height. It is this larger barrier height which actually controls leakage current in the device. The height of this barrier can be optimized through geometry and junction depth choices.

A second way of understanding this effect is to follow the electric field lines as they emanate from the gate and go to the corner. They begin to diffuse and spread out in the oxide and continue to do so in the semiconductor. Thus there is a weaker link between the surface potential in the semiconductor and the gate voltage in the corner region.

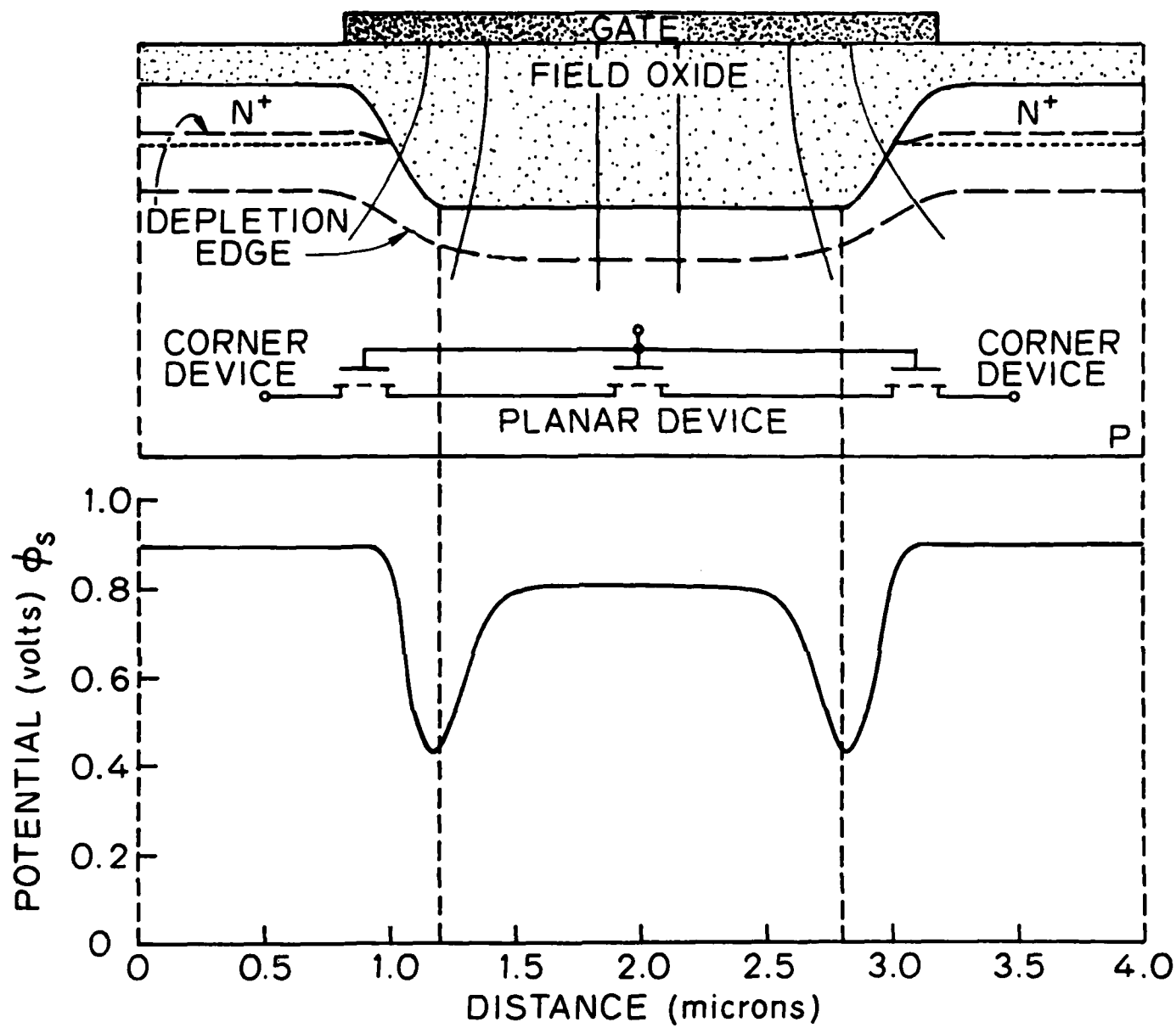
The device physics at the corner allow the entire isolation region to be modeled by three devices whose channels are in series, two corner devices and a planar device. Because of the corner geometry, the corner device has a flatter subthreshold slope and a higher threshold voltage, and thereby controls the current flowing in the isolation device. For the isolation structure to be modeled like this, the channel must exist around the corner and be controlled by the gate. Hence, the metallurgical boundary as well as the depletion region of the junctions must lie above the corner.

The curvature of the oxide/semiconductor interface at the corner plays a major role in the corner effect. In a device with a small oxide radius, the control of the surface potential by the gate voltage is reduced. This is because it is difficult for the electric field to reach into the corner. The addition of a back gate bias enhances the corner effect. The additional gate voltage required for the extra band bending changes the surface potential less at the corner than at the planar region, and hence enhances the corner effect.

An analytical development has been done of the device physics of isolation structures that exhibit the corner effect. The oxide capacitance of the corner was determined by conformal mapping techniques and the MOS 1D equations were solved in cylindrical coordinates. This allows a better understanding of the dependence of isolation on various structure parameters.

With our understanding of the corner effect, we have designed and made a set of masks that enable us to verify the corner effect experimentally. Devices of varying channel lengths and widths have been fabricated using the laboratories here, including the Canon FPA 1431 projection-alignment system purchased under JSEP support in FY78.





$$V_G = 18 \quad V_S = 0 \quad V_D = 0 \quad V_{SUB} = 0 \quad N_A = 2 \times 10^{16} \text{ cm}^{-3}$$

DEVICE WITH CORNER EFFECT

Figure 1-19: Cross-Section of chip with corners of oxide exposed

The first two process runs were made on  $\langle 110 \rangle$  oriented silicon wafers with a KOH etch to produce vertical sidewall grooves that are later oxidized to form the field oxide. Initial experimental results on these devices verified the basic benefits of the corner effect. To solve some processing difficulties and to use a fabrication process similar to current industrial techniques, two more process runs were made on  $\langle 100 \rangle$  oriented silicon wafers with plasma etching to produce the trenches. Different etching gases and oxidations produced structures with three different interface radii.

Figure 1-20 shows the subthreshold characteristics of four typical devices. All have channel widths of  $500\text{ }\mu\text{m}$  and channel lengths of  $7.5\text{ }\mu\text{m}$  on the mask. The oxide thickness is 6400 angstrom and the substrate was implanted with boron to increase the surface doping to  $1.3 \times 10^{16}\text{ cm}^{-3}$ . They were measured with  $V_{ds} = 0.05\text{ V}$  and  $V_{sub} = 0.0\text{ V}$ . Curve A is from a transistor whose source/drain junctions have been driven in below the oxide corner and thus obeys simple one dimensional MOS equations. Curve B corresponds to the structure which had the largest corner radius of the fabricated devices (Figure 1-21). It displays a slightly flatter subthreshold slope and higher threshold voltage compared to A. The transistor which had a slightly smaller interface radius has the subthreshold characteristics of curve C. Because its interface radius is smaller, the resulting subthreshold curve is flatter than the previous two curves. The fourth subthreshold curve, labeled D, corresponds to the structure which had the sharpest corner of all the fabricated devices (Figure 1-22). As a result the subthreshold curve is much flatter than the previous curves and the isolation is significantly improved. Between devices A and D, there is about a factor of two improvement in isolation where isolation is defined as the gate voltage needed to produce  $1\text{ pA}/\mu\text{m}$  of channel width of leakage current. Clearly the effect of technology on electrical isolation can be significant.

The structural variation of these latter three (in Figure 1-20) is a decreasing interface radius at the corner. The subthreshold slope becomes flatter as the corner radius is reduced, thus providing better isolation. For this device:

$$V_{ds} = 0.05\text{ V}, V_{sub} = 0\text{ V}, W = 500\text{ }\mu\text{m}, L = 7.5\text{ }\mu\text{m}, t_{ox} = 6400\text{ angstrom}, N_{sub} = 1.3 \times 10^{16}\text{ cm}^{-3}.$$

The top layer (in Figure 1-21) is the polysilicon gate. The region on the left, under the thin oxide, is the  $N^+$  source. This structure had the largest interface radius of the fabricated devices.

This structure (in Figure 1-22) had the smallest interface radius of the fabricated devices. The top layer is the polysilicon gate. The region on the left, under the thinner oxide, is the  $N^+$  source.

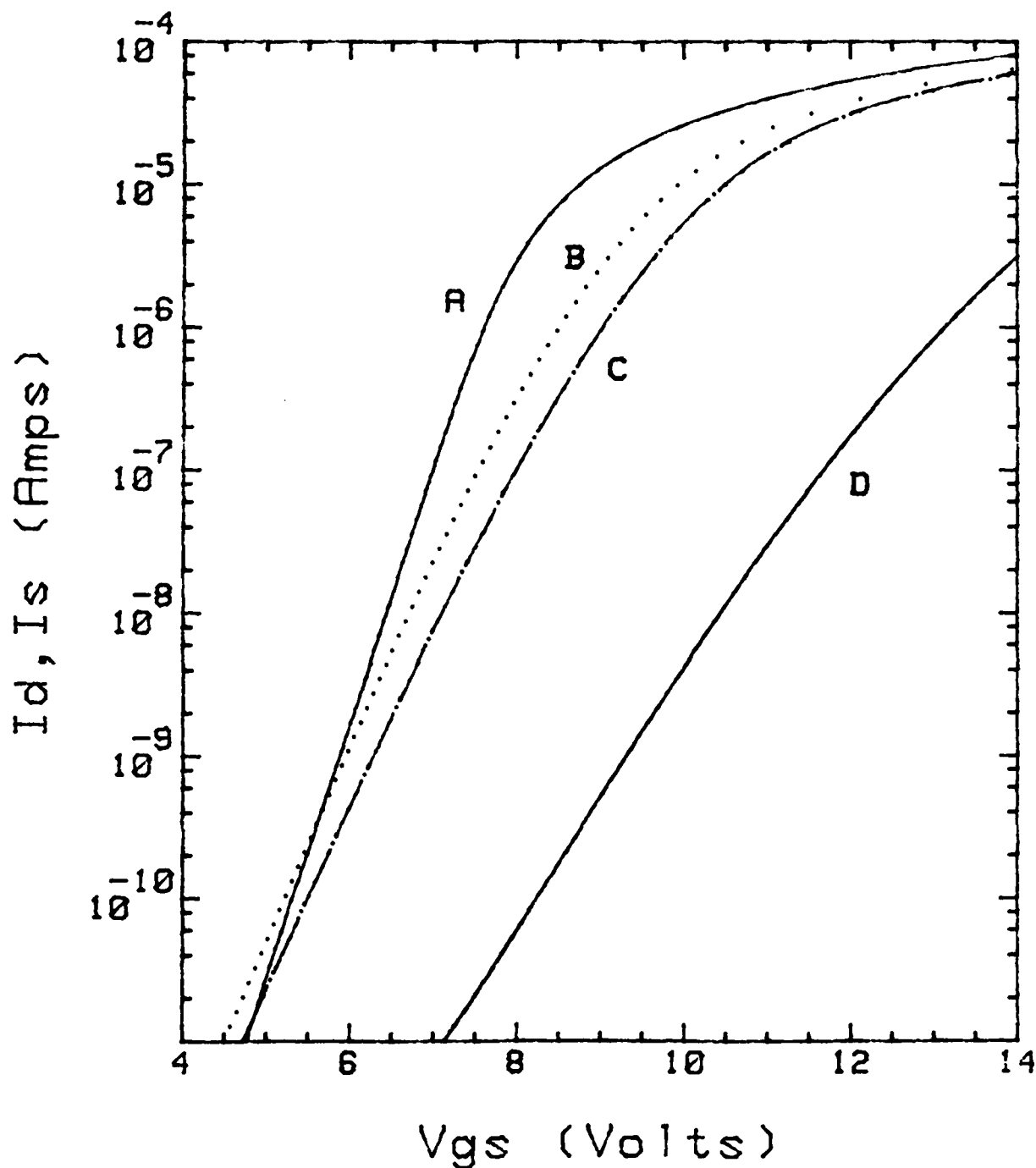
$W=500$   $L=7.5$ 

Figure 1-20: Typical example comparing a device without the corner effect (A) to ones with increasing amounts of the corner effect (B,C, and D)



### 1.2.2.3 Summary of Results

By computer simulations, an important two dimensional corner effect has been identified and investigated. This effect is a controlling potential barrier near the source of a device at the corner of the oxide, which is due to the reduced linkage between the gate voltage and the surface potential. The barrier results in dramatic improvements in isolation. A more complete article describing the physics of trench-like devices has been published [2]. Devices have been fabricated which verify this effect experimentally.

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In *1982 IEDM Technical Digest*, pages 2294-2297. IEEE, 1982.
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Trench Isolation Technology and Device Physics.  
to be presented at IEEE VLSI Symposium, Maui, Hawaii, Sept. 1983.

### 1.2.3 ELECTRONIC PROPERTIES OF POLYSILICON

*Investigators:* D.B.Kao, K.C.Saraswat

#### 1.2.3.1 Scientific Objectives

The objectives of this study are:

1. To investigate the electronic structures of grain boundaries in polysilicon by controlling the amount of incorporated atomic hydrogen through hydrogen implantation.
2. To investigate the effects of polysilicon gate in the annealing of oxide charges in the MOS structure.

#### 1.2.3.2 Background

*A. Electronic Properties of Polysilicon* The electrical properties of polysilicon are dominated by the grain boundaries which are the interface between two crystalline grains with different orientations [5, 3]. The lattice irregularities and dangling silicon bonds give rise to localized energy states. These states can trap mobile carriers and become charged. The charged localized states give rise to depletion regions, and a potential barrier which impedes the conduction of mobile carriers. Understanding the electronic structures of the localized states in the grain boundaries is, therefore, the key to controlling the conductivity in polysilicon.

Atomic hydrogen has been known to passivate dangling bonds, and reduce localized states [4, 2]. Hydrogen anneal of MOS transistors is a standard processing step. Hydrogenation is necessary in the fabrication of devices in amorphous silicon. Because hydrogen reduces localized states and makes possible effective dopant incorporation. Resistivity and optical properties of polysilicon are also affected by hydrogen.

To investigate the detailed electronic structures of grain boundary localized states, we need to precisely control the amount of hydrogen. We propose to implant hydrogen into devices fabricated in polysilicon, and measure the electrical properties of these devices. By measuring the density of localized states in polysilicon capacitors with different amounts of hydrogen, we hope to determine the energy distribution of localized states. By varying the amount of hydrogen and dopant concentration in polysilicon resistors, we can measure the effects of localized states on the conductivity of polysilicon.

*B Annealing of Oxide Charge in Poly-gate MOS structures* The thermal oxidation of Si results in fixed charges,  $Q_f$ , in the oxide near the Si-SiO<sub>2</sub> interface. This positive charge is a consequence of the oxidation process and is probably related to an intermediate Si-O bond state near the interface.

As shown by Deal, et al [1], this charge can be significantly reduced by a high temperature annealing in an inert ambient subsequent to the oxidation step.

Traditionally, this anneal is performed in situ immediately following the oxidation step to minimize  $Q_f$  in the final devices. However, the final value of  $Q_f$  is sensitive to subsequent processing. In particular,  $Q_f$  increases if the oxide is exposed to an oxidizing ambient at a sufficient temperature to allow oxygen to diffuse to the interface and start the oxidation process. This condition can easily occur during the withdrawal of wafers from the annealing furnace if  $O_2$  is allowed to backstream into the tube.

Polysilicon gate has a significant advantage over Al gate in that polysilicon forms a barrier to oxygen over the oxide and can be heated to effective  $Q_f$  anneal temperature ( $>900^\circ\text{C}$ ). Assuming that  $Q_f$  annealing is a relaxation process and that multilevel structure introduces no stress effects,  $Q_f$  should anneal in a polysilicon gate MOS structure independent of previous process history. In addition, subsequent high temperature exposures to oxidizing ambients should have no effect on  $Q_f$ .

### 1.2.3.3 Progress

#### A. Electronic Properties of Polysilicon

Electrical measurement of the devices fabricated in undoped polysilicon revealed some interesting results. The resistivity of undoped polysilicon is about  $10^6 \Omega\text{-cm}$ . The threshold voltage of PMOS with undoped polysilicon channel is about -8 volts. Both these results are in agreement with published data in the literature. C-V measurements show that polysilicon plays different roles in a capacitor, depending on whether it is attached to the top plate, bottom plate, or is part of the dielectric. I-V characteristic of polysilicon diodes and FET's shows great differences from their single crystalline counterparts.

These preliminary results not only verified the correctness of our process and mask design, they also offer encouraging clues which could lead to better understanding of the electronic properties of polysilicon.

#### B. Annealing of Oxide Charges

We have fabricated capacitors with  $\text{POCl}_3$  doped polysilicon gate on n and p type silicon wafers with 700 angstrom oxides grown in dry  $O_2$  at  $1000^\circ\text{C}$ . Selected wafers were given additional anneals in Ar,  $N_2$ , and dry  $O_2$ , for different lengths of time. The C-V results showed that  $Q_f$  was uniform for all wafers independent of the type of annealing. Since all wafers received an effective anneal during the

30 min 950°C  $\text{POCl}_3$  doping cycle, it is concluded that this anneal was sufficient to reach the minimum  $Q_f$  value. In other words,  $Q_f$  fully anneals during normal post poly-Si deposition processing and it is not necessary to reduce  $Q_f$  before this step.

#### 1.2.3.4 Summary of Results

MOS transistor, p-n diodes and resistors have been fabricated in undoped polysilicon and their electrical characteristics have been studied to understand the electronic properties of grain boundaries.

MOS capacitors with  $\text{N}^+$  polysilicon gate have been fabricated and their annealing behavior in oxidizing and inert ambients has shown that the fixed oxide charge  $Q_f$  is independent of the ambient for a polysilicon gate.

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### 1.2.3.7 Future Plans

#### A. *Electronic Properties of Polysilicon*

We need theoretical models for MOS capacitors with polysilicon as part of the top plate, bottom plate, or part of the dielectric. By analyzing the change of charges with applied voltages, we hope to determine the proper capacitor structure, polysilicon doping, polysilicon and oxide thicknesses, etc for the measurement of grain boundary states. We will also be able to determine whether high-frequency or quasi-static C-V measurement would yield sufficient information, and whether other measurement techniques, such as DLTS, should be considered.

Once the device structure and measurement techniques are determined, we will try to determine the grain boundary state distribution with implanted hydrogen. We will then try to correlate it with the conduction mechanism in the polysilicon resistors and MOSFET's, and generation-recombination in polysilicon diodes.

#### B. *Annealing of Oxide Charges*

We have shown that polysilicon gates stabilize oxide charges against annealing conditions. However, there is still a question concerning peripheral  $Q_f$  generated by the diffusion of oxygen at the edge of the gate which will be important for total  $Q_f$  control in small MOS devices. To investigate this edge effect of polysilicon gate, we have designed a set of capacitor masks for our Canon projection aligner. Some capacitors are comb-shaped with fingers as narrow as  $1.25\ \mu\text{m}$ . Others will have square holes of different sizes and densities. We will start processing these devices under different annealing conditions, and hope to gain some quantitative results and more insight into the anneal of oxide charges.

#### 1.2.4 OHMIC SEMICONDUCTOR CONTACTS WITH LOW MINORITY-CARRIER RECOMBINATION VELOCITY

*Investigator:* R.M.Swanson

##### 1.2.4.1 Scientific Objectives

Our research is directed toward the development of metal silicon contacts with low minority-carrier recombination velocity.

##### 1.2.4.2 State of the Art

The thin diffused layers in today's microelectronic circuits are generally transparent to minority carriers. As a result, the properties of many devices, particularly bipolar transistors, are partially controlled by recombination at the metal/semiconductor interface. Future projections of device geometries indicate that such recombination will assume greater importance in the future. An emitter junction cannot be made too shallow, or contact recombination will reduce its efficiency; making it deep, however, minimizes basewidth controllability and decreases speed because of emitter charge storage.

Reducing the minority-carrier recombination velocity at the metal/semiconductor interface would enhance device performance. Such an effect has been observed wherein current gain was greatly increased in polysilicon emitter transistors when a thin  $\text{SiO}_2$  layer was introduced. It appears that this gain was realized because of the differential tunneling probability between electrons and holes in thin  $\text{SiO}_2$  layers and, therefore, is limited to NPN transistors.

##### 1.2.4.3 Progress

Using the test structures developed during the last reporting period, device runs were initiated to quantify the tradeoffs between  $J_0$  reduction and parasitic series resistance when the oxygen content and thermal annealing parameters are varied. The test results indicate that for a SIPOS contact on a prediffused emitter structure (.07 to 1.2  $\mu$  deep; surface concentration less than  $10^{20} \text{ cm}^{-3}$ ), the  $J_0$  improvement is less than a factor of two when the oxygen content is varied from the lowest (10 - 20% atomic) to the highest (50 - 60% atomic). This insensitivity to the bulk film stoichiometry admits of at least two possibilities. The minority carrier transport may be insensitive to the bulk composition if the interfacial and adjacent regions limit transport; however a more likely explanation is that bulk recombination in the diffused emitter due to either SRH or AUGER mechanisms is beginning to dominate. These emitter profiles which are transparent when a metal contact is used become opaque when the  $J_0$  is reduced to the  $10^{-14} \text{ A/cm}^2$  region. From a practical standpoint, since the specific contact resistance as measured with a TIM test structure increases from  $2 \times 10^{-6} \text{ ohm-cm}^2$  to  $10^{-4}$

ohm-cm<sup>2</sup> for the low and high oxygen content films, and since there is no significant attendant improvement in the emitter  $J_0$ , the low oxygen content films are to be preferred in structures that utilize a prediffused emitter structure. It should be noted, however, that this resistance may be of advantage in structures that require a series ballast resistance to improve operating stability.

SIPOS as deposited is highly defective and requires a high temperature anneal to activate the dopant species; presumably, a concurrent annealing of associated defect structures improves minority carrier transport properties; yet, too high an annealing temperature will cause excessive outdiffusion from the highlydoped SIPOS layer into the monocrystalline region. A comparison of SIPOS contacted devices annealed for thirty minutes at 900 and 1000°C displayed a drastic increase in  $J_0$  (by a factor of 10) for the higher anneal temperature. Spreading resistance profiles indicate that while the emitter-base junction depth was unaltered, the surface concentration was enhanced by outdiffusion from the SIPOS to a level where the emitter had lost its transparency and the resulting  $J_0$  displayed only marginal improvement over the control metal contacted device. Studies to determine the minimum anneal temperature required are under way.

The optimal structure envisioned for the SIPOS contact relies only on the outdiffusion from the SIPOS into the underlying monocrystalline silicon to form the emitter base junction. This junction should be as shallow as possible to minimize the bulk recombination in the monocrystalline region yet should present enough of a barrier to reduce the minority carrier population at the SIPOS-Si interface. A device incorporating the low oxygen concentration SIPOS in this type of structure has yielded a  $J_0$  of  $1.8 \times 10^{-14}$  A/cm<sup>2</sup> (corrected to 300°K), the lowest of any yet measured. Comparisons of films with varying oxygen content and thermal annealing treatments in this configuration have not yet been completed.

A reliable metallization scheme remains to be devised to protect these films from the aluminum which is currently used as the contact metal. Pd has been found to yield consistently low resistance contacts to monocrystalline silicon. In the application to SIPOS the silicide will form only if the oxygen content is low. This indicated the necessity for an intervening capping layer of oxygen free polysilicon, despite the additional complications that this presents to the modeling of these structures. If this is insufficient to ensure the integrity of these films, a barrier layer, perhaps of Ti/W may have to be added.

#### 1.2.4.4 Summary of Results

SIPOS contacts have been developed that yield nearly two orders of magnitude decrease in emitter saturation current and have, at the same time acceptable series resistance.

#### 1.2.4.5 Recent Publications

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Technology and Performance of SIPOS Heterojunction Emitters.  
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Conference Held at Ft. Collins, CO.

#### 1.2.4.6 Future Plans

The work to date has established the feasibility of a low surface recombination velocity contact utilizing SIPOS for  $N^+$  structures at DC. Before application to high speed switching bipolar devices can be considered, there are several fundamental issues which need to be resolved. The dynamical response of the films at high frequencies is unknown, as is their behavior at elevated temperatures. Although the  $J_0$  values are reproducible in these test structures, their consistency and long term reliability in a VLSI fabrication environment need to be examined. The behavior of complementary  $P^+$  contacts is also unknown. Finally the fabrication of devices entirely in SIPOS (analogous to the case in POLY) is a consideration for applications to VLSI where SIPOS would play the role of polysilicon with oxygen content as an additional design variable.

### 1.2.5 SUBMICRON DEVICE PHYSICS AND TECHNOLOGY: Silicide:Si Interface including Effects Of and On Oxygen

*Investigators:* I. Lindau and W. E. Spicer

#### 1.2.5.1 Scientific Objectives

The thrust of our part of the JSEP program is investigation of Si interfaces. As reported previously, we have found that oxygen and other contaminants play a key role in determining the properties of interfaces between Si and the silicides which are becoming so important for VLSI. The thrust of the results reported here is in understanding such complex interactions with oxygen. In order to produce a sufficient background to understand this work, it is essential to understand the systematics of the formation of the silicides on Si and the interface thereof. Such work is also reported here.

In recognition of the very large instrumentation expenditure necessary for this work and the necessity in using working teams of three or four researchers at Stanford Synchrotron Radiation Laboratory (SSRL) where it is necessary to run experiments 24 hours a day for periods as long as several weeks, there was a large advantage in combining the JSEP with ARO and DARPA support for given projects. We will indicate such combinations. It should be emphasized that in all cases the JSEP funds allowed for expansion of the work played a critical role in obtaining the results reported here.

#### 1.2.5.2 Progress

##### *1. Interaction of Oxygen with Silicon d-metal Interfaces*

We have carried our synchrotron radiation photoemission measurements from both the valence states and the core levels of Si<111>/Cu, Ag, Au and Pd interfaces, before and after exposure to  $30 \times 10^6$  L of oxygen at room temperature. In all cases, the oxygen interacts with the Si and not the metal, and the Si oxidation rate is much higher than that for a clean Si<111> surface. The strongest oxidation enhancement is obtained with Cu and Pd. For noble metal overlayers, the interaction with oxygen produces the growth of a SiO<sub>2</sub>-like phase having a Si-2p chemical shift of  $\sim 3.8$  eV; this is in direct contrast to clean Si<111> which cannot be oxidized to form SiO<sub>2</sub> under the same conditions. This implies that the noble metal disrupts the Si sp<sup>3</sup> hybrids at the Si surface with a consequent increase in the Si reactivity. This behavior rules out models in which noble metal atoms absorb onto the surface forming an atomically abrupt interface with the Si.

This work was also supported by Army DAAG29-82-K-0087 and the work reported herein was performed at SSRL which is supported by DOE, Office of Basic Energy Sciences; and NSF, Division of Materials Research.

## *II. The Si/Rare Earth Metal Interface*

We have studied the Yb/Si and Cu/Si interfaces using Synchrotron Radiation UPS, XPS and Auger Electron Spectroscopy. The electronic structure was monitored as a function of both metal coverage and subsequent annealing cycles.

In contrast to the narrow, inactive interface observed at room temperature, the annealed Yb/Si interface is quite reactive, with 6 min. heating at 300°C being sufficient to completely react a 500 angstrom Yb metal overlayer on Si. The reaction is more rapid at 500°C. The two annealing temperatures produced two distinct compounds with compositions YbSi and YbSi<sub>2</sub>, respectively (corresponding to known bulk stoichiometries for this system).

These compounds are mixed valent, with the Yb metal atoms being in both 2+ and 3+ charge states. The fact that the Yb 4f emission moves toward and appears to cross the Fermi level after reaction supports valence fluctuation rather than inequivalent lattice sites as the explanation for this behavior.

This work was also supported by DARPA-ONR N00014-79-C-0072 and the work reported herein was performed at SSRL which is supported by DOE, Office of Basic Energy Sciences; and NSF, Division of Materials Research.

## *III. Detailed Study of Role of Ag in Enhancing Oxygen Reaction with Si*

As mentioned above, it has been found that Ag (as well as other metals) enhanced oxygen uptake on Si and changes the nature of the oxygen band, i.e. only "sub-oxides" of Si are found on pure Si at room temperature but with only sub-to-monolayer quantities of metal, SiO<sub>2</sub> is formed and the reaction rate is much larger. In order to understand this phenomenon on an atomic scale we are studying the position of the Ag when evaporated on Si in sub to monolayer quantities using the SEXAFS technique. We find that appreciable amounts of Ag are located just beneath the Si surface and believe that this is important in explaining the change of oxidation properties. This work is continuing.

This work was also supported by ARO (DAAG 29-82-K-0087). The work reported was performed at SSRL which is supported by DOE and NSF.

### 1.2.5.3 Summary of Results

The Si-oxygen chemistry at room temperature can be drastically changed by noble and transition metals of interest for VLSI. This is particularly important for silicide formation where oxygen at the silicide:Si interface can have unfortunate effects on the key electronic characteristics.

It has been established that the rare earth metal, Yb, forms the silicides YbSi and YbSi<sub>2</sub> at moderately high temperatures (YbSi at 300°C and YbSi<sub>2</sub> at 500°C). Much has been learned about the chemistry and electronic structure of these materials. However, it is important to realize that this opens up a new class of silicides - the rare earth silicides - which are conceivably very important for VLSI. It is important that this work be followed up appropriately; however, resources to do so appear to be strikingly lacking. Thus, it is questionable whether or not such follow-up will occur.

### 1.2.5.4 Recent Publications

#### Journal Papers

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Photoemission Investigation on the Oxidation of Si(111)-Ag Interfaces and Its Relation to  
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in press.

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Mexico, 25-27 January 1983, To Be Published in *J. Vac. Sci. Technol.*

### 1.2.6 INTERACTION OF ARSENIC AND OTHER IMPURITIES WITH SILICON SURFACES AND INTERFACES

*Investigators:* S.C. Perino, M.A. Taubenblatt, C.R. Helms

#### 1.2.6.1 Scientific Objectives

In the past periods, the objective of this part of the program was to determine the effect of arsenic and boron on the electronic structure of the silicon free surface. These results were then compared to structures in silicon integrated circuits where high interfacial dopant concentrations are present due to interfacial segregation. One of our current objectives was to complete this investigation. This major objective has been accomplished with the completion of the PhD dissertation of S.C. Perino entitled "The Electronic Structure and Deposition Kinetics of Arsenic on the Silicon Surface" [6] which was supported by this program.

With this investigation completed, we began a study of the effect of surface cleaning procedures on the electronic structure and chemistry of the Si surface. The major objective for this period was to determine the effect of the steps in the RCA cleaning procedure on the composition of the Si surface region.

#### 1.2.6.2 Progress

*Introduction:* The initial stages of materials growth in IC processing can be critical in determining their ultimate physical and electrical properties. Often, this initial growth is dependent on surface preparation and contaminants present on the substrate material. There are many examples. The density of stacking fault defects in epitaxial material depends strongly on the presence of contamination induced nucleation sites for these defects. [2] Nucleation of whisker growth can occur due to the presence of transition metals. [4]. The breakdown characteristics and uniformity of thin  $\text{SiO}_2$  layers can be adversely affected by the presence of carbon on the surface at the onset of oxidation. [5] Thus, the importance of understanding the nature and role of surface contaminants on these and other IC processes cannot be underestimated.

In this part of the research program, we have thus far investigated the composition and thickness of contaminants on Si as a result of various chemical cleaning procedures, and the interface properties of ultra-thin thermally grown  $\text{SiO}_2$  layers. These studies have been made employing Auger spectroscopy, sputter profiling, and ellipsometry.

Carbon and Oxygen are found to be the two main surface contaminants, with their relative amounts distinctly dependent on the chemical cleaning procedure used. These results are in agreement with



those of a previous study. [7] In the growth of thin thermal  $\text{SiO}_2$  layers, previous models [11] have indicated that interface width is dependent on the thickness of thermal  $\text{SiO}_2$  grown. However, our studies indicate that this effect is purely an artifact of the sputtering process and that the  $\text{SiO}_2/\text{Si}$  interface width is nearly constant during the early stages of oxide growth.

**Measurement Techniques:** The characteristics of these thin films were determined using Auger spectroscopy, sputter profiling, and ellipsometry. Auger spectroscopy provided information about the chemical composition of the surface layers down to the 0.1% level. Three techniques were used to measure the film thickness:

1. escape length of Auger electrons,
2. sputtering time to the interface, and
3. ellipsometry.

Due to escape length effects, the chemical shifts of the KLL and LVV Auger transitions for Si and  $\text{SiO}_2$  can be used to determine the thickness of the oxide. The Auger signal strengths for Si and  $\text{SiO}_2$  can be used to determine the thickness of the oxide. The Auger signal strengths for Si and  $\text{SiO}_2$  are given by:

$$S_{\text{Si}} = e^{-d/L}$$

$$S_{\text{SiO}_2} = A \times (1 - e^{-d/L})$$

where  $d$  = oxide thickness,  $L$  = escape length (3.5 angstrom at 90eV and 28.5 angstrom at 1600eV at an average angle of  $42^\circ$ ), and  $A = 2$  = sensitivity factor.

The LVV transition is useful in the range 0-10 angstrom, and the KLL transition in the range 5-50 angstrom.

Thicknesses from sputter times were obtained using a predetermined sputter rate from thicker  $\text{SiO}_2$  samples, measured with ellipsometry. This technique was limited to films greater than 10 angstrom, and was employed mainly with the thicker thermal oxides.

Ellipsometry is a widely used technique to measure the thickness and refractive index of thin films, provided the substrate refractive index is known. For ultra-thin films (<100 angstrom) however, the results obtained are highly dependent on the substrate refractive index, and incorrect values of this index can lead to erroneous measurements of the thin film parameters. Typical ellipsometer measurements on silicon are made using a value of  $3.85 - 0.02i$  for  $n_s$ . The imaginary part is

determined from bulk absorptivity, and does not really characterize the surface region where the ellipsometry measurement is made. A study [10] has shown that the substrate refractive index near the surface is dependent on the surface treatment. Thus it is necessary to use a value of  $n_s$  which is appropriate for the surface region in evaluating ellipsometry measurement of very thin films.

We have determined the substrate surface refractive index directly with ellipsometry, by making a measurement within 10" of removing a silicon substrate from an HF 50:1 dip and DI water rinse. The possible contamination accruing from this exposure was later determined to be <3 angstrom. The index obtained in this manner was 3.85-0.1i, and ellipsometry results obtained using this value, over the range 10-200 angstrom, were in substantially better agreement with the other two techniques employed. Using the "bulk" value for the silicon refractive index, thicknesses obtained were approximately 15 angstrom greater than with the measured index. Figure 1-23 compared the results of these three techniques.

For films < 20 angstrom, it can be shown [1] that  $\Psi$  is almost insensitive to the film thickness,  $x$ , and that  $d\Delta/dx$  is nearly constant with respect to film thickness, and over a wide range of film refractive index (1.4-2.5). Using this result, one can determine the film thickness by the following equation:

$$x = (\Delta_{\text{subs}} - \Delta_{\text{film}}) / (d\Delta/dx)$$

This ellipsometric method was used for the native oxide studies, with film thicknesses < 20 angstrom.

#### *Composition of surface contaminants, and the effect of chemical cleaning*

The term "native oxide" has long been used to describe the thin film contamination of silicon surfaces, as observed using ellipsometry, and having a thickness of 20-40 angstrom. Our studies of this native oxide indicate that this film is not more than 10-20 angstrom, and in most cases is less than 10 angstrom, and, that the film thickness and composition is strongly dependent on the cleaning procedure used.

Samples analyzed were as received from the wafer manufacturers, after an HF 50:1 dip, and at times following this (3hrs and 3 days), and at various stages of the RCA cleaning procedure. The thicknesses determined by Auger escape lengths, and ellipsometry disagreed by 2-5 angstrom. This is clearly more than would be expected from error analysis, and may be due to inhomogeneities in the surface layer.

The wafers (Wacker n-type, <100>) as received, measured 10 angstrom, using the ellipsometric technique described earlier (i.e. compared to a just HF etched surface.) After an HF dip followed by 3

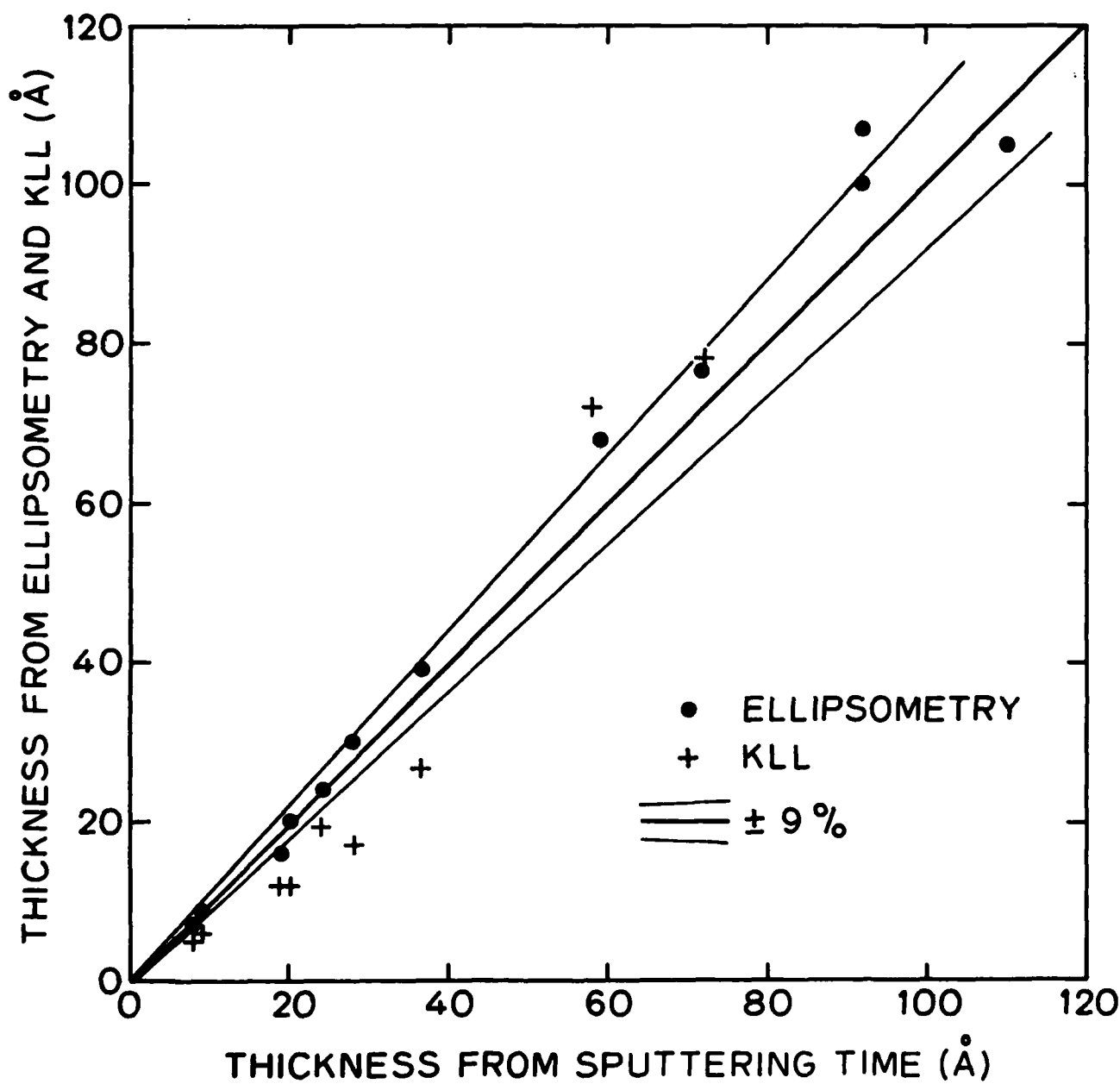


Figure 1-23: Comparison of Thicknesses Determined by Ellipsometry, Sputtering Time and KLL Auger Line Ratios

hours in air, the surface layer had increased to 3 angstrom, and after 3 days to 17 angstrom. Auger analysis indicated that the as received wafers had a thickness of 8 angstrom, with a composition of 2.8ML (monolayers  $\approx 10^{15}$  atoms/cm<sup>2</sup>) oxygen, and 0.15ML carbon, with trace amounts of nitrogen (0.01ML) present. Samples loaded into the analysis chamber 15' after a HF 50:1 etch, showed a quite

different surface layer. These samples had a 3 angstrom surface layer (as determined by Auger) made up of 0.4ML oxygen, and 1.0ML carbon.

The significant change in the amount of carbon present on these two samples led us to investigate the effects of various stages of the RCA cleaning procedure. These results are shown in Table 1-8.

Table 1-8: Effect of Various Cleaning Procedures

Procedure			Oxygen Concentration	Carbon Concentration
(1)	As received	-----→	2.8 ml	0.2 ml
	↓			
(2)	H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub>			
	↓			
	DI Water			
	↓			
(3)	NH <sub>4</sub> OH:H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	-----→ air	2.3 ml	0.5 ml
	↓			
	DI Water			
	↓			
(4)	HCl:H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O			
	↓			
	DI Water	-----→	2.1 ml	0.1 ml
	↓			
(5)	HF Dip → DI → H <sub>2</sub> O <sub>2</sub> → DI	-----→ air	1.1 ml	0.2 ml
	↓			
	Air			
	↓			
	DI Water	-----→	0.4 ml	1.0 ml

Two important points should be noticed. At step 4, the wafer has undergone treatment to remove carbon compounds and heavy metals from the surface, but not  $\text{SiO}_2$ . In addition, the  $\text{H}_2\text{O}_2$  present in the solutions causes a thin layer of  $\text{SiO}_2$  to form at the surface. The surface layer at this point comprises a significant amount of  $\text{SiO}_2$  (6 angstrom), with very little carbon present (0.1ML). A similar result can be obtained after a HF etch (which previously resulted in large amounts of carbon), by now not allowing contact with air, and instead exchanging the HF solution for DI water,  $\text{H}_2\text{O}_2$  and back to DI water.

These results show that exposure to air is the source of carbon contamination in the case of the HF etch, and that a clean  $\text{SiO}_2$  layer prevents the carbon from sticking. The  $\text{SiO}_2$  layer thus acts as a passivating layer with regard to other surface contaminants.

In Si oxidation studies it is shown that uniformity and breakdown improve if the final HF dip is omitted [5], which, we show, results from a much reduced carbon concentration at the initial surface.

*Interface evolution during thermal oxidation.* The nature of the  $\text{SiO}_2/\text{Si}$  interface has become increasingly important as IC circuit dimensions are reduced. Previous Auger sputter profiling studies of ultra-thin  $\text{SiO}_2$  layers [11] have shown that thinner layers result in a reduction of the measured interface width. This result was explained by an intrinsic property of oxide growth, in which interface roughness increases with oxide thickness. In this study, we show that this effect is an artifact of the sputtering process, and that the interface width is unchanging with regard to oxide growth for oxides greater than 10 angstrom [9].

That the sputtering process causes interface broadening is well known. Furthermore, deposited energy can be related to a sputter induced diffusion coefficient [8, 3]. However, because the damage energy causing the broadening is spatially distributed, the effect is greatly reduced in thin oxides. This can be seen in Figure 1-24. For a thicker oxide layer the entire energy distribution will sweep past the interface as the sample is sputtered, with the total broadening equal to the summed energy deposited at the interface, namely the area under the curve. But for thin oxides, much of the energy is initially deposited beyond the interface, so that the summed energy is much less.

This model has been applied to the measured interface widths of  $\text{SiO}_2/\text{Si}$  samples which have all been grown to identical starting thicknesses, and etched back chemically to various thicknesses [9]. A number of different sputtering gasses and energies have also been used. The results are shown in Figure 1-25.

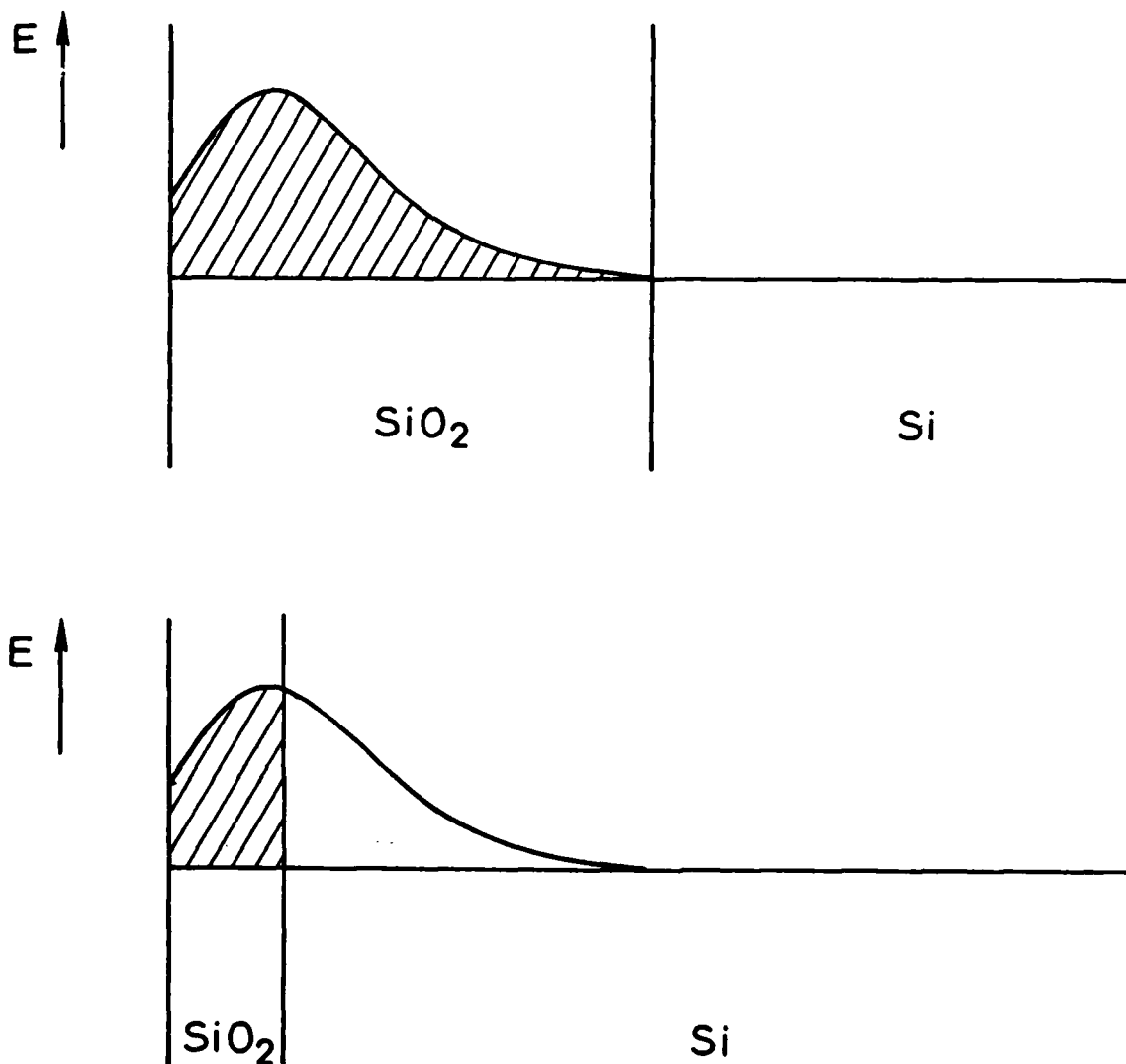
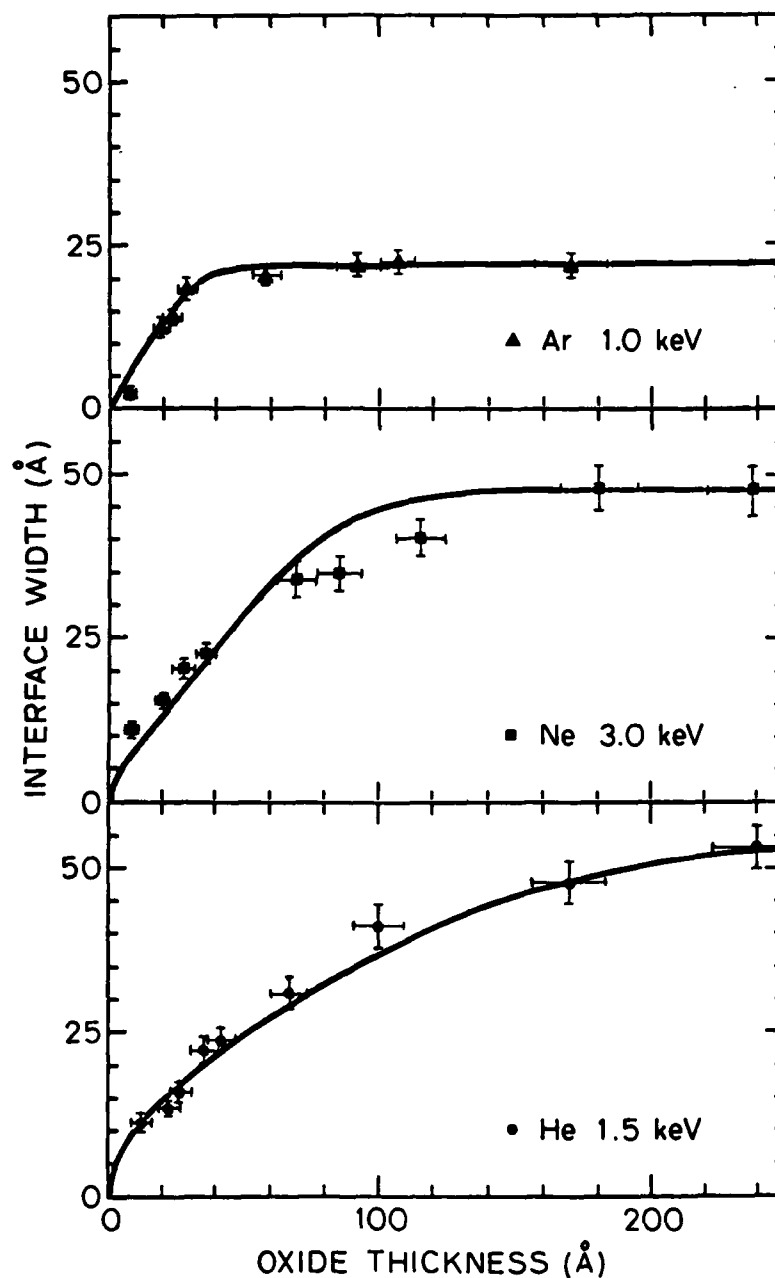


Figure 1-24: Schematic Diagram of the Spatial Distribution of the Ion Energy Distribution for Thick and Thin SiO<sub>2</sub> layers on Si.

The data are a reasonable fit to the theory, and since there was no variation in thermal processing of the samples, one can conclude that the grown oxide thickness is not a factor in determining the interface width. When this effect is factored out of the data presented in reference [11] for oxides grown to different thicknesses, one finds that the interface width remain nearly constant.



**Figure 1-25:** Theoretical Curves vs. Experiment. Interface Width is that due solely to ion knock-on broadening, Auger escape length and an intrinsic width (10 angstrom) have been removed

### 1.2.6.3 Summary of Results

In addition to the completion of our previous work on the Interaction of arsenic with the silicon surface, significant progress has been made in our studies of the effect of cleaning procedure on the chemistry and electronic structure of silicon surfaces.

One major result is that carbon is a dominant contaminant on the silicon surface after immersion in HF containing solutions. In addition, a previous finding [11] that the Si-SiO<sub>2</sub> interface is rough for thin thermal oxides was proven to be an artifact of the measurement technique.

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### 1.2.7 INTERCONNECTIONS FOR HIGH DENSITY, HIGH PERFORMANCE VLSI

*Investigators:* R.F.W. Pease and P. de la Houssaye

#### 1.2.7.1 Scientific Objectives

One result of the increasing scale of integration is that the packing density and performance of VLSI circuits is now limited by interconnects and not by the intrinsic speed of active devices. One result of scaling to finer dimensions in accordance with normal scaling rules is that the current density in the interconnects increases as dimensions are reduced. This can lead to serious problems with electromigration in metal conductors and this problem might well become more serious as minimum dimensions are scaled down and as the scale of integration is increased. However, studies on electromigration in aluminum/copper interconnects has led to the interesting discovery that under certain conditions the mean time to failure (MTF) actually increased as the conductor widths dropped below  $2\text{ }\mu\text{m}$  [3]. This was attributed to the fact that under the specific deposition conditions for that material the grain boundaries in conductors of widths below  $2\text{ }\mu\text{m}$  extended normally across the cross section of the conductor (i.e. perpendicularly to the direction of current flow); thus in the transmission electron microscope (TEM) the conductors had a "bamboo" appearance. Similarly sized conductors deposited under different conditions failed to show the bamboo structure or the increased MTF [4]. Pierce and Thomas have reported that furnace annealing (following deposition) can bring about the required bamboo structure but such growth was not reproducible [1]. The goal of this project is to see whether the techniques in selective electron (or laser) beam annealing [2] can be used to bring about the bamboo structure in metallization systems which do not normally show such a structure and whether such treatment leads to increased mean times to failure.

#### 1.2.7.2 Progress

The first phase of the project was to find a way of revealing the grain structure of the Al/Cu metallization without the need to prepare the sample for inspection in the TEM. A variety of etchants were investigated, the only one showing even marginal promise was a 10:1 water:HF solution saturated with molybdic acid ( $\text{MoO}_3$ ). However the results were insufficiently positive to warrant further effort and phase contrast or dark field optical microscopy of undecorated samples was felt to be adequate for our initial work.

The second phase was to carry out preliminary experiments to determine electron beam parameters suitable for annealing I.C. metalization. A beam current of  $20\text{ }\mu\text{A}$ , beam diameter of  $3\text{ }\mu\text{m}$  and an electron energy of  $20\text{ keV}$  was predicted to be suitable and this indeed proved to be the case.

Figure 1-26 shows a  $4\text{ }\mu\text{m}$  metallization line on an I.C. structure before beam annealing (but after

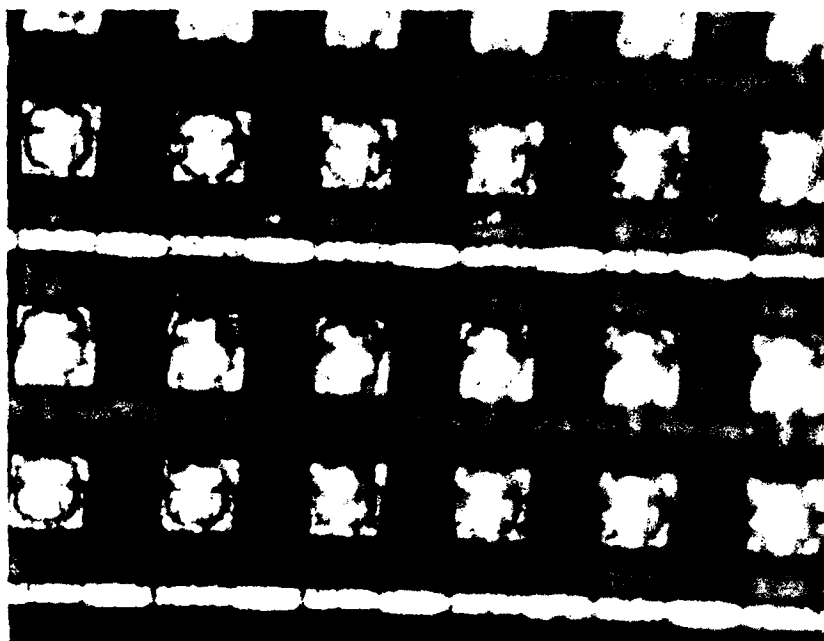


Figure 1. Portion of chip before e-beam anneal. Note random pitting of the surface of the Al (horizontal) lines. X1000, optical microscope.

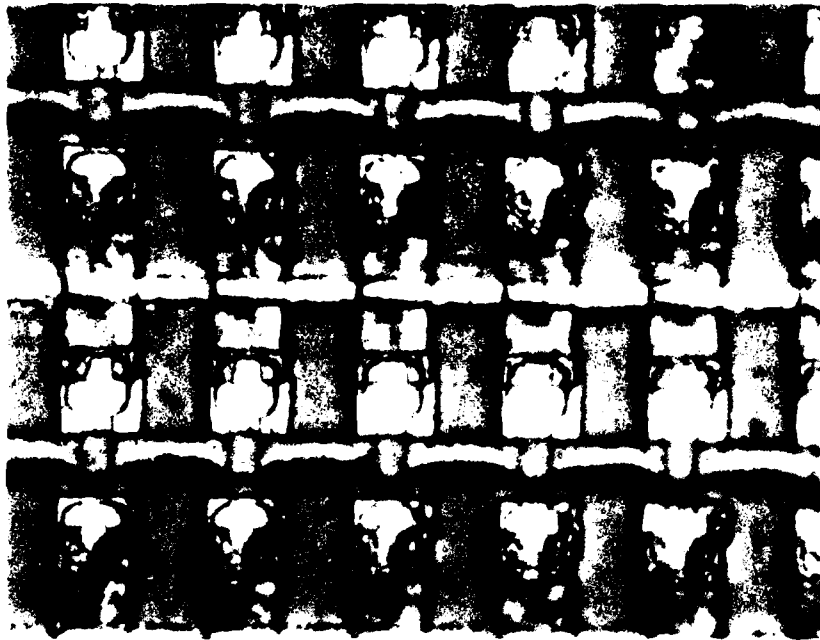


Figure 2. After exposure with e-beam (20 keV, 20  $\mu$ A current, beam-diameter  $\approx$  3  $\mu$ m). Scan direction is vertical. Note the metal has been remelted in places along the scan direction. X1000, optical microscope.



Figure 3. Chip area with 30  $\mu$ A exposure. Metal lines have been melted away. X1000, optical microscope.

## 2. INFORMATION SYSTEMS

### 2.1 Real-Time Statistical Data Processing

*Principal Investigator: T. Kailath*

#### 2.1.1 Scientific Objectives

The goals of this research program were to develop optimal and suboptimal schemes for estimating the location of radiating sources by a passive array.

#### 2.1.2 Progress

##### 2.1.2.1 Optimal Schemes

In [7] we derived the Maximum Likelihood (ML) estimator of the locations of *multiple source*, for the general setting of *partially correlated* sources. This setting includes the important practical problem of *multipath propagation* as a special case.

The structure of the ML processor obtained allows physical interpretation of the estimator, and reduces, as expected, to the Hahn and Tretter (1973) processor for the case of a single source. It is shown that the ML processor consists of a bank of beam-formers, each focused to a different source, followed by a variable matrix-filter that is controlled by the assumed locations of the sources. In the special case of uncorrelated sources and very low signal-to-noise this processor reduces to an aggregate of ML processors for a single source, with each processor matched to a different source.

It should be noted that the implementation of the ML estimator requires knowledge of the *number* of the sources as well as their *spectral density* matrix. Because of this and because of the computational complexity of the algorithm it is recommended only as an "offline" procedure, following a suboptimal scheme as the one described next.

##### 2.1.2.2 Suboptimal Schemes

In [5] and [8] we presented a *new approach* to the problem of source location. This approach is *nonparametric*, and hence *robust*, and can cope with *multiple, partially correlated, sources*. The important problem of *multipath propagation* is thus included as a special case.

It is shown that the *eigenstructure* of the *spectral-density* matrix of the received signals contains *all* the information on the sources. Algorithms for estimating the *number* of the sources, their *locations*,

and their *spectral-density* matrix have been derived. Simulation results that illustrate the performance of the proposed method have been presented (see Figure 2-1 for an example). In Figure 2-1, two sources at locations  $(-1,5)$  and  $(10,20)$  impinge on an array with three sensors at  $(1,0)$ ,  $(0,1)$  and  $(0,0)$ . The signal-to-noise ratio is 20db. The two sources have overlapping spectra of bandwidth 0.05 centered at 0.25.

The proposed method can, obviously, be applied also to the special case of direction-of-arrival estimation of *wideband* sources. For the even more special case that the sources are *narrowband*, a more efficient algorithm has been derived. In [6] and [9] we have shown that for this 2-D harmonic retrieval problem, all the information is contained in the eigenstructure of the *spatio-temporal covariance* matrix of the received signals. Algorithms for estimating the *number* of sources, their *frequencies*, their *directions-of-arrival*, and their *covariance* matrix have been derived, and their performance illustrated by simulation.

It should be noted that the new eigenstructure based methods we have derived are extensions of the methods of Schmidt [4] and Bienvenu [1](see also Reddi [3]), which are themselves extensions of the pioneering work of Pisarenko [2].

### 2.1.3 Summary of Results

1. Derivation of the ML estimator of the locations of multiple partially correlated sources, and the corresponding Cramer-Rao lower bound.
2. A new eigenstructure-based approach to the problem of estimating the number, locations and spectral-density matrix of multiple partially correlated *wideband* sources.
3. A new eigenstructure-based approach to the problem of estimating the number, frequencies, direction-of-arrival, and covariance matrix of multiple partially correlated *narrowband* sources.

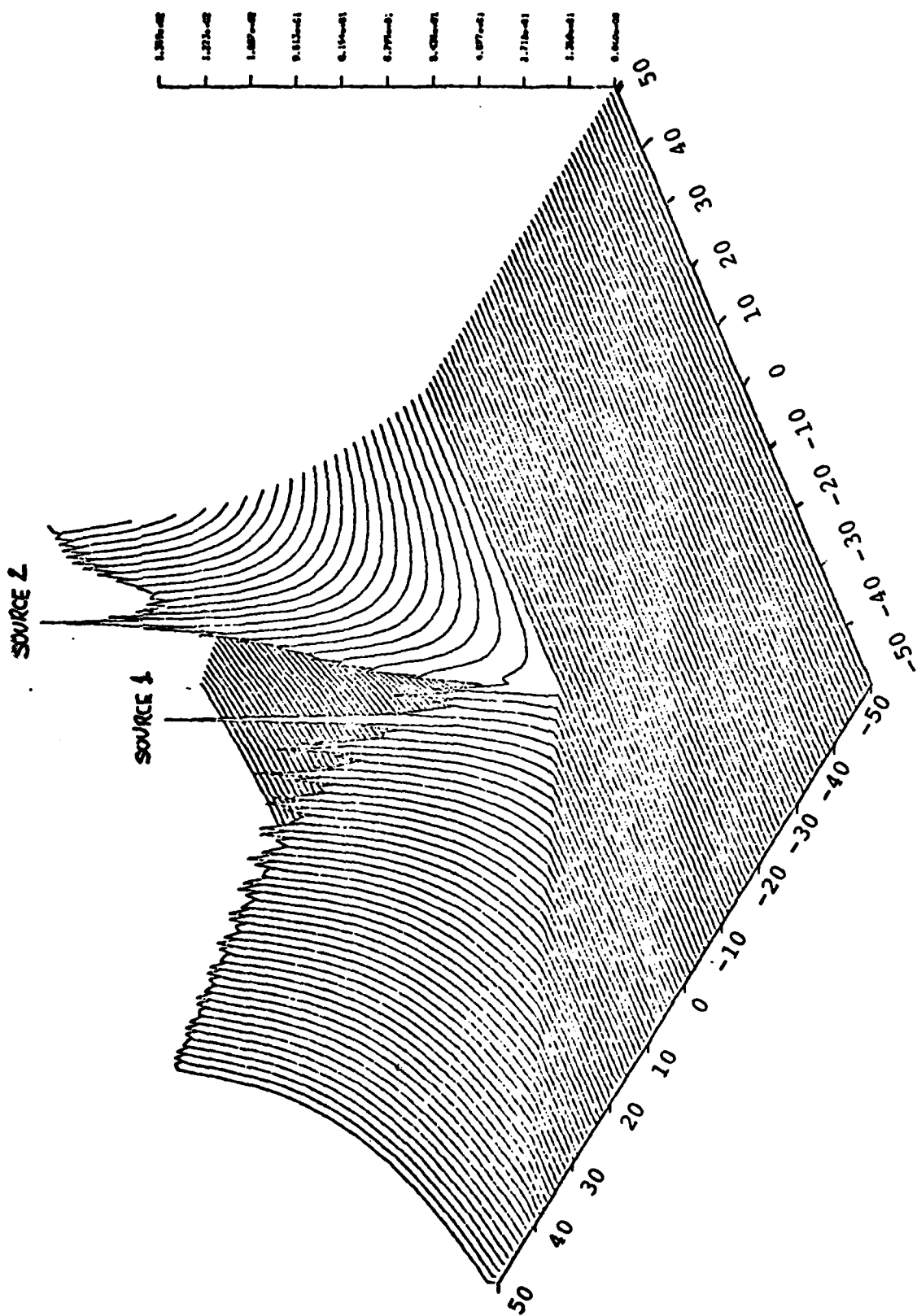


Figure 2-1: Simulation Results



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- [1] Kwon, W.H., Bruckstein, A.M., and Kailath, T.  
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*Int. J. Control* 37(3):631-643, March, 1983.

- [2] Reddy, V.U., Egardt, B., and Kailath, T.  
Least-Squares Type Algorithm for Adaptive Implementation of Pisarenko's Harmonic Retrieval Method.  
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- [3] Samson, C.  
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*Optimal Control, Applications & Methods* 3:389-397, 1982.
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A Unified Treatment of Fast Algorithms for Identification.  
*Intern'l. Journal of Control* 35(5):909-934, May, 1982.

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- [1] Citron, T.K., Kailath, T. and Reddy, V.U.  
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In *Intern'l. IEEE Conference on Acoustics, Speech and Signal Processing*. IEEE, Paris, France, May, 1982.
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In *Intern'l. IEEE Conference on Acoustics, Speech and Signal Processing*. IEEE, Boston, MA, April, 1983.
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Covariance Eigenstructure Approach to 2-D Harmonic Retrieval.  
In *Intern'l. IEEE Conference on Acoustics, Speech and Signal Processing*. IEEE, Boston, MA.,  
April, 1983.

#### Accepted Journal Papers

- [1] Egardt, B., Kailath, T. and Reddy, V.U.  
High-Resolution Spectral Analysis Using Multi-Step Adaptive Prediction.  
to be published in *Circuits, Systems, and Signal Processing*.
- [2] Kailath, T., Ljung, L. and Morf, M.  
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to be published in *IEEE Trans. Autom. Contr.*, vol. 28, no. 6, June 1983.
- [3] Kailath, T. and Ljung, L.  
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Lattice Filter Parametrization and Modeling of Nonstationary Processes,  
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Covariance Eigenstructure Approach to Detection and Estimation by Passive Arrays, Pt. I: Direction-of-Arrival and Frequency Estimation of Multiple Narrowband Sources.  
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#### Dissertations

- [1] Delosme, J.-M.  
*Algorithms for Finite Shift-Rank Processes.*  
PhD thesis, Information Systems Laboratory, Department of Electrical Engineering, Stanford University, August, 1982.
- [2] Lashkari, K.  
*A New Deconvolution Technique for Periodically Excited Systems.*  
PhD thesis, Information Systems Laboratory, Department of Electrical Engineering, Stanford University, March, 1982.

#### Invited Presentations at Conferences

1. IFAC Symposium on Digital Control, Delhi, India, Jan. 5-7, 1982.
2. Large Scale Systems & Signal Processing Workshop, Bangalore, India, January 12-16, 1982.
3. SIAM Conference on Applied Linear Algebra, Raleigh, North Carolina, April 26, 1982.
4. State Space Estimation Course, NASA-Langley, Washington, D.C., June 16-17, 1982.
5. IEEE International Symposium on Information Theory, Les Arcs, France, June 21-25, 1982.
6. American Mathematical Society, Annual Summer Meeting, Toronto, Canada, August 23-27, 1982.

#### Seminars

1. Indian Institute of Technology, Bangalore, India, January 1982.
2. Tektronix, Beaverton, Oregon, February 5, 1982.

3. Fairchild Semiconductor, Inc., Palo Alto, CA, March 19, 1982.
4. University of California, La Jolla, CA, April 8, 1982.
5. Arizona State University, Tempe, AZ, April 9, 1982.
6. Kuwait University, Kuwait, April 15, 1982.
7. Cairo University, Egypt, April 21, 1982.
8. Department of Statistics, Stanford University, May 25, 1982.
9. University of Maryland, MD, June 18, 1982.
10. McMaster University, Canada, August 24, 1982.

## 2.2 FAST ALGORITHMS AND VLSI ARCHITECTURES

*Principal Investigator: M. Morf*

### 2.2.1 Scientific Objectives

The objective of this work was the development of fast algorithms that are suitable for implementations in VLSI based architectures. The algorithms considered have a wide range of applications from matrix computations for general and special structured matrices (e.g. Toeplitz, Hankel, and related matrices, as well as banded, rational and sparse matrices.), to real-time signal processing, high-resolution spectral estimation, source location, signal detection, analog and digital communication, CCCI, estimation, control, to radar, sonar and lidar.

### 2.2.2 Progress

Our research effort under JSEP support during this period has been summarized very well in the two theses and a paper which are described in the sections below; we are very pleased to report this work since it contains several major break-throughs in this research area.

#### 2.2.2.1 Contributions to the Analysis and Modeling of Multichannel Autoregressive Stationary Processes

*Investigator: Mohamed T. Hadidi*

Details of this work can be found in [1].

Autoregressive modeling of stationary processes has many applications in signal processing, examples being data compression prior to transmission, and spectral estimation via the maximum entropy method (MEM). In contrast to the scalar case, it is well known that some structural features of multichannel autoregressive stationary processes remain hidden or not fully exploited in available multichannel algorithms.

In this thesis we present new results dealing with various aspects of modeling and analysis of multichannel autoregressive stationary processes, which bring to bear more of the structure of such processes than has previously been the case. Thus we give a fast algorithm which constructs a ladder model from an AR one in  $O(p^6 N^2)$  operations, where  $p$  and  $N$  are the process dimension and its order respectively. We believe this algorithm to be the most efficient among existing ones for this problem. We also derive new formulas expressing the covariance matrix of a multichannel autoregressive stationary process (in general a block Toeplitz matrix) in terms of either of its

predictors. Previously, both of the predictors had to be used for this purpose. Finally we provide a structural proof of the generalized Barnett factorization for bezoutians of square matrix polynomials (such as the predictor polynomials), which adds to the structural insight gained through the first two results.

At least one of the results in this thesis was attempted to be solved by many people at least for *ten years*, up to this point envain.

#### 2.2.2.2 Algorithms for System Identification and Source Location

*Investigator: Arye Nehorai*

Details of this work can be found in [2].

This thesis deals with several topics in least squares estimation and applications to *high accuracy source location*, an important problem. It begins with a derivation of a mapping between Wiener theory and Kalman filtering for nonstationary autoregressive moving average (ARMA) processes. Applying time domain analysis, connections are found between time-varying state space realizations and input-output impulse response by matrix fraction description (MFD). Using these connections, the whitening filters are derived by the two approaches, and the Kalman gain is expressed in terms of Wiener theory.

Next, fast estimation algorithms are derived in a unified way as special cases of the Conjugate Direction Method. The fast algorithms included are the block Levinson, fast recursive least squares, ladder (or lattice) and fast Cholesky algorithms. The results give a novel derivation and interpretation for all these methods, which are efficient alternatives to available recursive system identification algorithms.

Multivariable identification algorithms are usually designed only for left MFD models. In this work, recursive multivariable identification algorithms are derived for right MFD models with diagonal denominator matrices. The algorithms are of prediction error and model reference type. Convergence analysis results obtained by the Ordinary Differential Equation (ODE) method are presented along with simulations.

Sources of energy can be located by estimating time differences of arrival (TDOA's) of waves between the receivers. A new method for TDOA estimation is proposed for multiple unknown ARMA sources and additive correlated receiver noise. The method is based on a formula that uses only the receiver cross-spectra and the source poles. Two algorithms are suggested that allow tradeoffs

between computational complexity and accuracy. A new time delay model is derived and used to show the applicability of the methods for non-integer TDOA's. Results from simulations illustrate the performance of the algorithms.

The last chapter analyzes the response of exact least squares predictors for enhancement of sinusoids with additive colored noise. Using the matrix inversion lemma and the Christoffel-Darboux formula, the frequency response and amplitude gain of the sinusoids are expressed as functions of the signal and noise characteristics. The results generalize the available white noise case.

#### 2.2.2.3 Recursive Identification Logarithms for Right Matrix Fraction Description Models

*Investigators:* A. Nehorai and M. Morf

This work is discussed in more detail in [3].

Multivariable identification algorithms are usually designed only for left matrix fraction description (LMFD) models. In this paper we consider recursive identification algorithms for right matrix fraction description (RMFD) models with diagonal denominator matrix. The algorithms are of prediction error (PE) and model reference (MR) type. Convergence analysis leads to a positive realness condition for the convergence of the MR algorithm to the true RMFD of the system. The PE scheme converges to a local minimum of the criterion with probability 1. Results from simulations illustrate the convergence of the algorithms.

One of the many applications of these algorithms are *Multiple Source Location*.

#### 2.2.3 Summary of Results

We are very pleased to report several major break-throughs in our research area. At least one of the results we obtained was attempted to be obtained by many people at least for *ten years*, up to this point in vain. Several new methods for identifying (multiple) source locations, even with correlated sources and receivers were derived and analysed. All these algorithms can be implemented directly or in ladder-forms via the use of our CORDIC based "*scattering*" array architectures very efficiently in VLSI based real-time computer systems.



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*Algorithms for System Identification and Source Location.*  
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*Recursive Identification Logarithms for Right Matrix Fraction Description Models.*  
Submitted to IEEE Trans. AC and 22nd CDC, Jan 1983.

#### 2.2.5 Recent Publications

The following publications were supported by JSEP and are the basis of our *other current work*; it will be reported in the next annual report.

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Technical Report M735-21, Information Systems Laboratory, Department of Electrical Engineering, Stanford University, June, 1982.
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*A Unified Stochastic Description of Efficient Algorithms for Second-Order Processes.*  
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## 2.3 Signal Processing and Compression

*Principal Investigators: R.M. Gray, M.E. Hellman, T.M. Cover, J.T. Gill*

### 2.3.1 Scientific Objectives

The objective of this project is to study the basic limitations on the performance and efficiency of communication networks, including both multiuser and point-to-point systems. A parallel objective is to develop improved methods of signal processing for these systems from the structures used to verify the performance limitations. Attention will be directed toward the trade-offs between performance and complexity in signal-processing algorithms. Signal processing for data compression, improved signal-to-noise ratios, and privacy will be investigated.

### 2.3.2 Progress

#### 2.3.2.1 Vector Quantization

*Investigator R.M. Gray*

During the indicated period one project was essentially completed and several new projects were initiated. Papers based on the projects completed during the previous JSEP contract year were published as detailed in a subsequent section.

In joint work with Professor H. Abut of San Diego State University and Mr. B. Tao of Hycom Inc., Irvine, CA, a real-time implementation of a full search vector quantizer (VQ) for speech waveforms using LSTTL and CMOS devices was completed. The system uses codebooks developed using the Linde-Buzo-Gray vector quantizer designed algorithm [8] to provide medium rate waveform coders operating at either 6500 bps and 13000 bps. Separate codebooks are used for voiced and unvoiced segments. This project demonstrated the feasibility of real-implementation of VQ's with codebooks of at least 8 bits per vector. It also has provided many suggestions for simpler and better quality implementations. A paper based on this project is currently being revised.

Preliminary results were obtained for a cascade vector quantization system consisting of a sequence of low bit rate VQ's, each quantizing the error remaining from the original signal to the reproduction determined by the previous VQ's in the cascade. The hope was to obtain simpler VQ's of a given rate (that is, VQ's requiring much less search effort for a codebook of a given size). The preliminary results were pessimistic and indicated that the quality is severely degraded by the suboptimal implementation and hence this structure is not a promising one for further research.

Preliminary results have been developed for another VQ structure with the potential for efficient implementation of large codebooks: a vector predictive quantizer or VPQ that operates as a predictive quantizer or DPCM system on vectors instead of scalars. While prediction accuracy is lost when predicting more samples ahead, it was felt that the possible gains by using VQ on the prediction error might more than compensate for the loss. Professor Allen Gersho of the University of California at Santa Barbara independently arrived at the same idea and was able to demonstrate the basic system was indeed capable of significant improvements over scalar DPCM. We have confirmed his results in our own experiments and are continuing to look at variations of such systems.

A new system for combined data compression and reliable channel communication was proposed based on a coupling of the data compression design algorithm of [8] with the joint source and channel coding theorem of Dunham and Gray [4] which showed that optimal codes for both data compression and channel communication could be obtained by designing an optimal data compression system using a modified distortion measure: the expected distortion over the noisy channel instead of the ordinary distortion. Preliminary results were obtained for simple Gaussian sources and binary symmetric channels. These results are optimistic and research on this project will continue.

#### 2.3.2.2 Advances in Cryptography

*Investigator:* M.E. Hellman

Our work covers several areas and is reported here by the area.

##### *1. Discrete Logarithms*

In [3] we presented a public key distribution system which depended on the difficulty of computing discrete logarithms. Merkle [9] and Adleman [1] have found a fast, subexponential method for computing this function. We have extended this algorithm from  $GF(p)$  to the more general case,  $GF(p^m)$ . In doing this, we also found a way to rigorize the use of a precomputation, by defining a "virtual spanning set". These results were presented at the IEEE Crypto '82 Conference, and a paper [6] has been submitted for publication.

The algorithm in [6] was developed for the case when  $p$  was fixed and  $m$  was tending toward infinity. It could not be used for the case when  $m$  was fixed and  $p$  was tending to infinity, for example, in  $GF(p^2)$ . Recently, we have found a new algorithm [5] for computing discrete logarithms over  $GF(p^2)$  that works for about 99.8% of values of  $p$ . This algorithm uses "quadratic fields" as the

appropriate algebraic structure to be used instead of the integers in the original Merkle-Adleman algorithm.

## *II. Coin Flipping by Telephone*

Two parties, A and B, might wish to agree on the result of a coin toss even though they are only conversing by telephone and neither can see the results of the other's tossing a coin. Even if the two parties do not trust each other and do not have the services of a trusted intermediary, it is possible for them to agree on the result of the toss.

[2] gives a protocol which solves the problem by using the method of "Oblivious Transfer". The method relies on the difficulty of computing square roots modulo  $N$ , where  $N$  is the product of two, large, secret prime numbers  $p$  and  $q$ . [11]'s "Mental Poker" approach can also be used.

We have developed a new approach [10] which requires only a normal one-way function, such as can be easily derived from the DES or any other conventional cryptosystem. The weaker requirements of our system make it simpler to implement and less likely to have a hidden weakness.

We have also been able to prove our approach is secure if the discrete logarithm problem is a one-way function. Our protocol also differs from the "Oblivious Transfer" in that no party can force himself to lose, or to reduce his chances of winning.

## *III. The First Repetition of a Pattern in a Symmetric Bernoulli Sequence*

We studied the expected number of bits in a random sequence before any  $l$ -bit pattern repeats. This problem was motivated by a recently adopted National Standard, of using the DES in an output-feedback mode, to achieve a synchronous cipher. Our result shows that the expected length of the sequence is on the order of  $2^{1/2}$ , and thus exposes a weakness of the encryption method. A paper [7] on the solution of the probabilistic method has been accepted for publication.

### **2.3.2.3 Multiple-User Communications and Information Theory**

*Investigator: T.M. Cover*

We are seeking a general theory for the data compression of several sources. To date we have concentrated efforts in how to allocate resources to the various data gathering nodes in order to obtain the data needed to arrive at the best decision (rather than how to process data that has already been gathered).

Progress has occurred in:

1. the multiple descriptions problem, and
2. compounding the growth of information

#### **2.3.2.4 The multiple descriptions problem**

A manager asks several data gatherers to go out in the field and gather data as best they can in order to contribute to his ultimate decision. If he says no more, then they will all independently arrive at the same idea and end up gathering the same data. This is totally redundant. Consequently, the manager must allocate the data gathering tasks.

Unfortunately, most allocation schemes have the undesirable property that the data gatherers can form no conclusions of their own because of the incoherence of the data they have gathered. For example, if asked to gather data on a given animal, one person might look at the tail and think it is a snake, another might look at the legs and think it is a tree trunk, and another might investigate the ears and think that the object is a tree. Only the central processor views it correctly as an elephant.

The theory of how to gather information about an object when each of the data gatherers must be able to arrive at a good decision and the central data gatherer must be able to arrive at a very good decision is covered by a series of papers including the paper by Cover and El Gamal. This paper puts forth a natural rate region for the problem. A converse has not yet been established.

#### **2.3.2.5 Compounding the growth of information**

Suppose that a central manager allocates his resources over several data gathering nodes. The resulting new state of knowledge should then lead to a different allocation of resources for the next stage of information collection. His information compounds. We are interested in maximizing the rate of growth of this information.

We believe that portfolio theory is intimately related to maximizing the rate of growth of information. In portfolio theory, one allocates a proportion of current capital to various stocks in the stock market, gets a return, reallocates the resulting capital and thereby compounds one's capital each investment period, in a manner analogous to the more general problem of gathering information (capital). This analogy is productive since a large collection of historical data is available to test the proposed approaches.

We are developing a theory that should have the implications that one can do as well in such compounding as if one knew ahead of time what the distribution for the stock market was. The

implications for data gathering would be that one can gather data in a stochastic environment in a sequential manner and do as well asymptotically as if one had known what the underlying distribution was. We would hope to develop a precise parallel between the portfolio selection problem and the data gathering problem and, from that, develop the appropriate results for the distributed data gathering question.

#### 2.3.2.6 Tree Compression

*Investigator: J.T. Gill*

Although the primary objective of this research has been the study of data compression methods of tree data (for example, expression trees that occur as the output of compilers for high level languages), we have obtained results in other related areas, including data compression for computer file systems.

For both tree data and one-dimensional data, we have concluded that variable length to fixed length coding schemes are more effective than fixed-to-variable schemes when the source statistics are unknown or are of high order. As an example, we applied both techniques to a large number of computer files: the variable-to-fixed scheme achieved a rate of 55% compared to 68% for the fixed-to-variable adaptive Huffman encoding.

We have investigated variable-to-fixed prefix encoding for ergodic Markov sources. Consider an irreducible Markov source that generates symbols from a source  $S$  according to a transition probability matrix all of whose entries are strictly positive. We have shown that a "greedy" variable-to-fixed encoding scheme asymptotically achieves the entropy lower bound on compression. Whether the coding scheme is truly optimum, not just in the asymptotic sense, remains an open problem.

The design of optimum codes for tree data is still an open problem; it is at least as difficult as the special case of linear (one-dimensional) data. However we have developed an efficient encoding algorithm for a special case of the problem. Given a finite collection of codewords and a string to be encoded, there is a dynamic programming algorithm that will find in linear time the optimum parsing of the string into codewords. We generalized this variable-to-fixed encoding procedure to the case where we want to compress parse trees by substituting abbreviations for commonly occurring subtrees (idioms). Given a collection of idioms (codewords), a linear-time dynamic programming algorithm can be used. The problem of selecting the best set of idioms remains open.

Work in data compression for computer files has continued. Our approach has been to attempt transparent file compression; that is, compression that requires no (or at most minor) changes to the computer operating system. This is accomplished by storing data on disks whose physical record sizes are actually smaller than the sizes that the operating system assumes. The data compression techniques studied are a combination of variations on Lempel-Ziv universal coding and variable-to-fixed encodings based on statistics gathered from the file systems. The data rate, based on a large sample of actual files, has ranged from 48% (for FORTRAN source programs) to 78% (for executable files). Based on these results, we propose to implement a prototype compressed file system with a physical record size of 1536 bytes versus a logical (operating system) size of 2048 bytes, for a data rate of 75%.

### 2.3.3 Summary of Results

A real-time hardware implementation of a vector quantizer for speech waveform coding based on LSTTL and CMOS devices was developed and studied. New projects on predictive vector quantization for waveform coding and computer aided design of combined data compression and noisy channel communication were initiated. Preliminary results for both new systems were promising and the projects will continue.

Our work is divided into several different areas:

1. *Discrete Logarithm* - We have developed a new algorithm for solving discrete logarithms over  $GF(p^{**2})$ .
2. *Coin Flipping by Telephone* - We have developed a new protocol that allows two mutually untrusting persons to flip a coin over telephone without the use of a third trusted intermediary.
3. *The First Repetition of a Pattern in a Symmetric Bernoulli Sequence* - We studied the expected number of bits in a random sequence before any  $l$ -bit pattern repeats.

We have put forth a rate region for the multiple descriptions problem which may turn out to be optimal. In any case, it is an information theoretic lower bound to what can be achieved. Also, we have results on the sequential allocation of resources, otherwise known as the stock market investment problem, which parallel the compound sequential Bayes decision theory work of Robbins, Blackwell and Hannan. Finally, we have proved that the maximum entropy spectral density estimate of Burg arises naturally as the limit of conditional probability densities.

Near optimal algorithms for variable-to-fixed encoding of both tree data and one-dimensional data have been developed. Simulations of transparent file compression have been performed, with the goal of an actual implementation of a compressed file system for a small computer.



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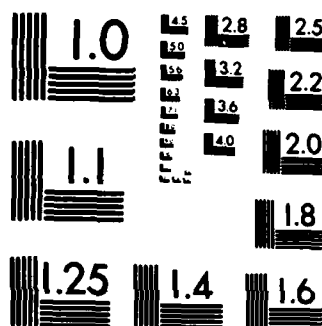
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